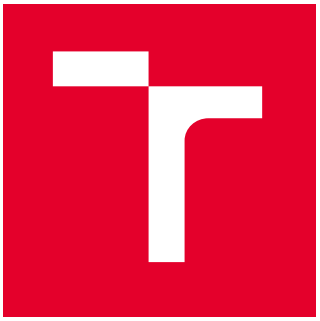

BRNO UNIVERSITY OF TECHNOLOGY

VYSOKÉ UČENÍ TECHNICKÉ V BRNĚ

FACULTY OF ELECTRICAL ENGINEERING AND COMMUNICATION

FAKULTA ELEKTROTECHNIKY
A KOMUNIKAČNÍCH TECHNOLOGIÍ

DEPARTMENT OF RADIO ELECTRONICS

ÚSTAV RADIOELEKTRONIKY

SELECTED PRACTICAL APPLICATIONS OF FRACTIONAL TWO-PORT SYSTEMS IN IMMITTANCE AND TRANSFER FUNCTIONS

VYBRANÉ PRAKTICKÉ APLIKACE FRAKTÁLNÍCH DVOJPÓLŮ V IMITANČNÍCH A PŘENOSOVÝCH FUNKCÍCH

DOCTORAL THESIS
DIZERTAČNÍ PRÁCE

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Abstrakt

Tato práce je rozdělena do pěti po sobě následujících částí (nepočítaje bibliografií). První část se zabývá představením implementace v navržené struktuře prvku s konstantní fázovou odezvou (constant phase element, dále jen CPE) založeného na sério-paralelním zapojení rezistorů a kondenzátorů. Následují rozbory vybraných zapojení pro implementaci takto navrženého CPE prvku a jejich možné srovnání s jinými zapojeními podobného typu v kapitole State of the Art. Cíle disertační práce, které byly stanoveny, jsou ve čtyřech bodech popsány v kapitole Objectives of Work. Úspěšnost plnění těchto bodů je pak probrána v závěrečné kapitole Concluding Discussion, společně s možností dalšího postupu implementací CPE prvků a jejich aplikace v obvodech. Hlavním bodem práce je druhá část Publications and Research sestávající se s publikovaných konferenčních článků a impaktovaných časopiseckých článků. Za zmínku stojí dva impaktované časopisy, pro publikaci v CSSP (Circuits, Systems, and Signal Processing), o tématu praktického návrhu RC aproximantů a jejich aplikace v CMOS konvejorech. Druhý článek, který měl nejsignifikantnější dopad na disertační práci byl publikován v impaktovaném časopise IEEE Access sestávající z problematiky elektronicky řiditelných a nastavitelných fraktálních filtrů. Obě navrhované aplikace v těchto impaktovaných časopisech nabízejí elektronickou ovladatelnost časové konstanty, hodnoty magnitudy a rekonfigurace. Čtenář bude seznámen s novými možnostmi použití CPE prvků v lineárních obvodech. Za účelem ověření prezentovaných konceptů byly u vybraných článků provedeny simulace v programu PSpice, stejně jako experimentální testy s vyrobenými čipy na pracovišti a s komerčně dostupnými prvky.

Klíčová slova

Konstantní fázový prvek (CPE), struktury neceločíselného řádu, proporční integrační a diferenční regulátor (PID, stejně tak $PI^{\alpha}D^{\beta}$), napěťový diferenční proudový konvejor, frekvenčně závislé prvky, celočíselné a neceločíselné integrace a derivace

Abstract

This dissertation is organized into five consequential sections (excluding the bibliography). The initial section delves into the introduction of the implementation in the proposed structure of the element with a constant phase response (Constant Phase Element, henceforth referred to as CPE), based on a series-parallel configuration of resistors and capacitors. This is followed by analyses of selected configurations for the implementation of the proposed CPE element and a possible comparison with other configurations of a similar type in the State of the Art chapter. The objectives of the dissertation are described in four points in the Objectives of Work. The success in fulfilling these objectives is then discussed in the Concluding Discussion, along with further possibilities of the implementation of CPE elements and their applications in linear circuits. The second part is the core of this dissertation, consisting of published

conference papers and articles in impact journals. Noteworthy are two impact journals for publication in CSSP (Circuits, Systems, and Signal Processing) on the topic of practical design of RC approximants and their application in CMOS conveyors. The second paper, which had the most significant impact on the dissertation, was published in the impactful journal IEEE Access and consists of issues related to electronically controllable and adjustable fractional filters. Both those proposed impact paper applications offer electronic control over the time constant, magnitude values, and reconfiguration. The reader will be introduced to new possibilities for the application of CPE elements. For the purpose of verification of the presented concepts, selected simulations were conducted in the PSpice program for some articles, as well as experimental tests with fabricated chips in the lab and with commercially available components.

Key words

Constant phase element (CPE), fractional-order dynamics, proportional integrational and differential controller (PID, also $PI^{\alpha}D^{\beta}$), voltage differencing current conveyor, frequency dependent elements, integer and non-integer integrations and derivations

DOMANSKÝ, Ondřej. Vybrané praktické aplikace fraktálních dvojpólů v imitančních a přenosových funkcích [online]. Brno, 2025 [cit. 2025-06-30]. Dostupné z: https://www.vut.cz/studenti/zav-prace/detail/161032. Dizertační práce. Vysoké učení technické v Brně, Fakulta elektrotechniky a komunikačních technologií, Ústav radioelektroniky. Vedoucí práce Roman Šotner.

DECLARATION

I declare that I have written the Doctoral Thesis titled “Emulators of immittances of higher orders and their applications” independently, under the guidance of the advisor and using exclusively the technical references and other sources of information cited in the thesis and listed in the comprehensive bibliography at the end of the thesis.

As the author I furthermore declare that, with respect to the creation of this Doctoral Thesis, I have not infringed any copyright or violated anyone’s personal and/or ownership rights. In this context, I am fully aware of the consequences of breaking Regulation §11 of the Copyright Act No. 121/2000 Coll. of the Czech Republic, as amended, and of any breach of rights related to intellectual property or introduced within amendments to relevant Acts such as the Intellectual Property Act or the Criminal Code, Act No. 40/2009 Coll., Section 2, Head VI, Part 4.

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Rád bych poděkoval mému vedoucímu práce Romanovi Šotnerovi za jeho přesný metodologický postup při práci na všech projektech, které mě při doktorském studiu potkaly. Bez jeho pomoci a schopnosti motivovat lidi kolem sebe by dokončení této práce nebylo možné. Bezesporu je tím nejlepším vedoucím, kterého jsem si mohl vybrat ke zdárnému odevzdání doktorské práce. Pokud bych měl někdy v budoucnu doporučit někomu vedoucího jeho bakalářské, magisterské nebo doktorské práce, bude to určitě Roman. Dále bych taky poděkoval všem kolegům UREL, za vytvoření kolektivu podporujícího přirozenou kreativitu a dobré podmínky ke studiu a práci.

Contents

PREAMBLE

Introduction

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1 Introduction

Fractional calculus is a branch of mathematical analysis that extends further development of the concept of differentiation and integration from integer orders up to real or complex orders. It provides a general framework for operations like differentiation and integration. The mathematical conception and the unconventional natural behavior of fractional calculus makes it a rich field for research, with potential applications still being explored in scientific and engineering disciplines, which have attracted increasing attention of researchers.

The historical background of fractional calculus is fascinating, as it goes back over several centuries, with early contributions from some of the most renowned mathematicians like Leibniz [1], Liouville [2], Riemann [3], Butzer [4] and many others [5], [6]. It was initially an only theoretical field, exploring the mathematical and extending knowledge of the traditional calculus. Despite its early establishment, the field remained largely theoretical until its potential was discovered in the late 20th century when there were many natural systems uncovered, which couldn't be accurately modeled by integer-order differential equations but could be described very efficiently by fractional-order differential equations. The recovery of interest in fractional calculus was fueled by the discovery of its applicability in modeling physical systems characterized by constant phase response. One of the first mention was in 1950 by Borisova and Ershler [7] following with more modern calculus statements [8], [9], [10], [11], [12].

As a fractional calculus evolved from a purely theoretical concept into a robust analytical tool, the evolution has seen its transition from complex mathematical constructs to a practical instrument of innovation and the shift in how scientists and engineers employ fractional calculus for modeling complex behaviors in their respective fields. With the continuous progression of research and the enhancement of computational capabilities, the future of the fractional calculus appears highly promising.

2 State of the Art

2.1 Fraction Calculus and Constant Phase Element

The RC network whose immittance is characterized by almost constant phase shift over an extended frequency range [13] (now so-called constant phase element - CPE) is a concept used in electrochemistry and impedance spectroscopy to model the frequency-dependent impedance element. Unlike an ideal capacitor, which has a frequency-independent capacitance that introduces a phase shift of exactly –90° between voltage and current (phase shift of 0° for resistor), a CPE can stand for the non-ideal behavior observed in real systems. A significant challenge in the practical implementation of CPE lies in its lack of commercial availability. However, in recent years, various substitutes for CPEs have been developed. These alternative solutions can be based on electrochemical components, as referenced in [14], [15], [16], organic materials as well as polymer composites [8], [17], [18], [19], [20]. Additionally, there has been progress in creating thick film layers composed of resistive, dielectric, and insulating materials on silicon substrates, as documented in [8], [20], [21]. The impedance Z_{CPE} of the ideally proposed CPE is:

$$Z_{CPE} = R_s + \frac{1}{j\omega C_s}, \tag{1.1}$$

where R_s and C_s stand for finial form of non-integer impedance and capacitance respectively, j is the imaginary unit and ω is the angular frequency response equal to $\omega = 2\pi f$. In our application this equation could be simplified for further development of CPE with custom phase deviation as [8], [12]:

$$Z_{CPE} = \frac{1}{Y_0(j\omega)^{\alpha}} \left[F^{1/\alpha} s^{(\alpha-1)/\alpha}\right], \tag{1.2}$$

where α is a proportionality of constant that represents the magnitude of the CPE. It's related to the capacitance in an ideal capacitor, α characterizes the phase order of the final CPE element. It varies in range from $\alpha \leq \pm 1$ and depends on phase shift φ ($\alpha = 1 - \varphi/90°$) [8]. Detailed description and discussion of the non-integer order passive two-terminal element can be seen in chapter Publication and Research under the Chapter A: *Practical Design of RC Approximants of Constant Phase Elements and Their Implementation in Fractional-Order PID Regulators Using CMOS Voltage Differencing Current Conveyors*, described in [8].

As previously discussed, there are several ways to create a CPE element that ensures a constant phase shift within a specified frequency range. For the purpose of this thesis, the most promising and frequently utilized structure will be the approximation of CPE through a resistor-capacitor configuration (RC [8], [11]). Detailed approximation of the serial-parallel structure can be seen on Figure 1. For more practical usage the mathematical foundation offers several approaches for approximation of CPEs [11], [12], [22], [23], aiming to achieve the desired bandwidth and phase ripple. These methods result in a specific distribution of zeros and poles (the roots of polynomial symbolical expression of impedance/admittance) related to the

previously mentioned passive RC sections [22]. The chosen approximation method and the calculation algorithm are detailed and further elaborated in [8]. In our case, the design of the CPE is based on the RC structure depicted in Figure. 1 is presented as an example. The final and corrected input admittance of the CPE can be expressed as [8], [22]:

$$Y(s) = sC_p + \frac{1}{R_p} + \sum_{i=1}^{m} \frac{sC_i}{sC_iR_i + 1}, \tag{1.3}$$

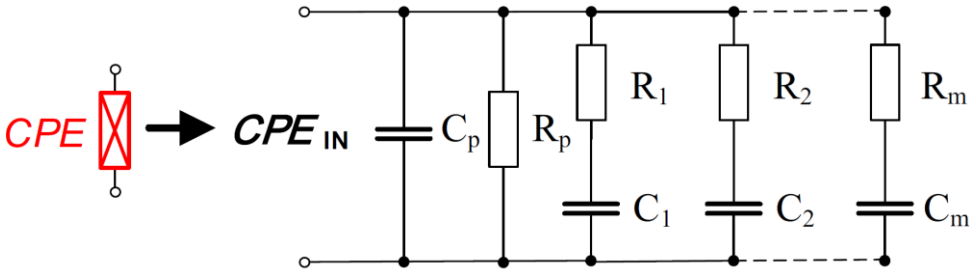

Figure 1. Scheme of an approximation of CPE by serial-parallel combination (branches) of RC segments [8]

Simulation results in Figure 2, demonstrating example of phase ripple and magnitude of a designed CPE, were obtained for specific values (selected example) of $\varphi = 30°$. Such a designed element is further used in Chapter A: *Practical Design of RC Approximants of Constant Phase Elements and Their Implementation in Fractional-Order PID Regulators Using CMOS Voltage Differencing Current Conveyors* [8].

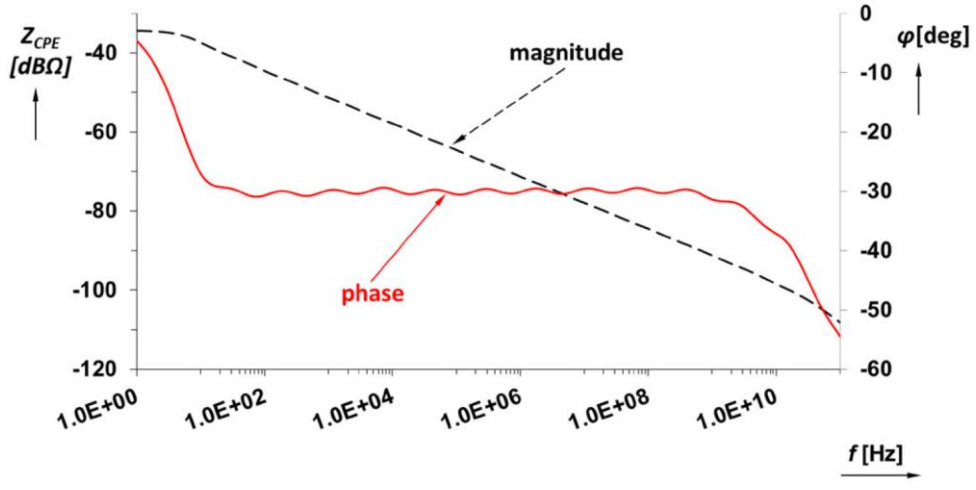

Figure 2. Simulation results of approximated CPE (exact values calculated in Chapter A: Practical Design of RC Approximants of Constant Phase Elements and Their Implementation in Fractional-Order PID Regulators Using CMOS Voltage Differencing Current Conveyors) for phase shift $\varphi = 30°$ and its magnitude [8]

2.2 Electronically Reconfigurable and Tunable Fractional-Order Two-Port Network

In numerous instances, the need arises for altering the transfer response (such as the type or bandwidth limit) in signal processing. However, just tunability or the ability to manual selection of the output often falls short of meeting these requirements, as pointed out in [24], [25]. The complexity of reconfiguring a filter's transfer response surpasses the capabilities of standard active devices like operational transconductance amplifiers [9]. This is because a broader spectrum of variables, including pass-band gain and pole frequency, are involved, as noted in [26].

2.3 Possible Application of Fractional-Order Filter

The solution of fractional-order (FO) circuits (as they are also stated in previous chapter 2.1) [12], [27], [28], [29], [30], introduces innovative features to this field. Unlike integer-order systems, FO circuits allow for the setting of area transition between stop-bands and pass-bands with a more gradual slope as referenced in [9], [27], [31], [32], [33] or as the example of the electronically reconfigurable fractional-order filter presented in Figure 3 and Figure 4. This unique feature arises from the magnitude slope's dependence on frequency, which is intrinsically linked to the order of the FO components employed in the circuit design, a concept further elaborated in [28]. More specific requirements on the slope of response of such a circuit can be fulfilled by applying FO approaches [34], [35], [36]. This property of FO circuits lays the groundwork for a more tunable and flexible approach to filter design and signal processing.

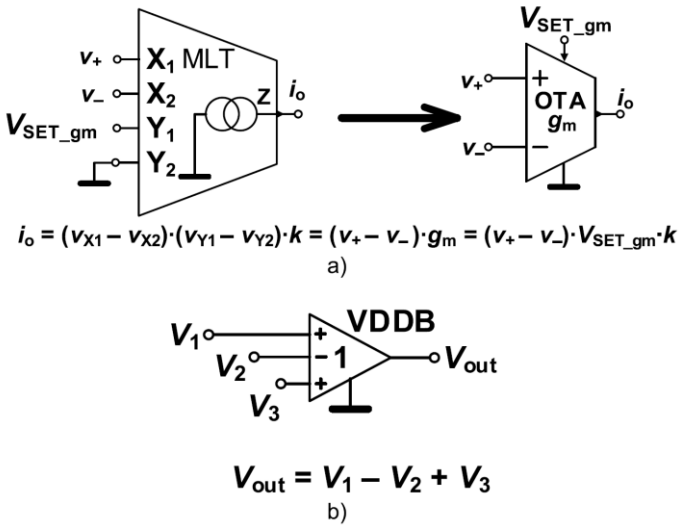

Figure 3. Possibility of configuration of active devices used for construction of the special fractional-order reconfigurable filter and its application: a) analog multiplier as OTA application, b) voltage differencing differential buffer [9]

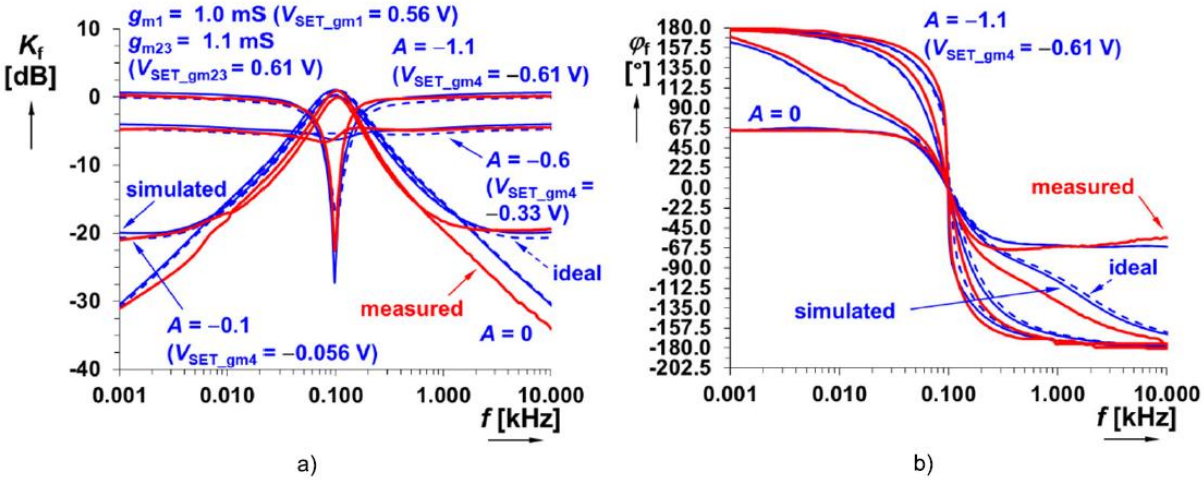

Figure 4. An example of possible frequency responses of a reconfigurable filter: a) magnitude responses, b) phase responses [9]

3 Objectives of Work

***Objective 1**: Initial research on the topic of fractional-order elements. Namely the design of a voltage and current controlled fractional-order PID regulator with reduced topology using known CPE design approach extended to more frequency decades. Following by the next specific part of this objective focuses to implementation of fractional-order behavior in the two-port design used in construction of complex analog systems (filters, controllers) especially for integer and fractional order response combination. The research question is: "What is the product of the sum of responses processed by integer and fractional-order path?".*

Recent designs of fractional-order PID regulators show significant lack of simple electronic variability and controllability of parameters, especially when standard operational amplifiers are used as active devices Chapter A. This subpart of this objective was partially fulfilled by a novel topology of PID using voltage differencing current conveyors (VDCC) and two CPE devices (structures and values adopted from Chapter A). The electronic adjustment allows simple time constant control by DC voltages and currents. There is an availability for implementing special CMOS active devices and circuit topology using only grounded passive elements (including CPEs). This fact is beneficial for possible integration of the complete device. The method as well as a complete algorithm of designing CPE element is described in Chapter A.

The second part of this objective consists of complex analog system and their integer and fractional order responses which they were not tested in previous works in literature in this specific form. The second authorship and the issues addressed regarding this topic are presented in Chapter B and Chapter C. Beyond fractional order elements, the reader can learn about practical solutions for the summing response of fractional and integer order differentiators, as well as a detailed Mathcad analysis of various functions. Results in Chapter B uses a summing block and two paths using independently adjustable voltage gains and including two different transfer responses (integrator, differentiator, two-port of higher order Chapter C) where each of them has an integer-order character and the second one has a fractional-order character. Presented results in 3D plots indicate very interesting and useful responses (especially for filtering applications, so-called inverse response filters Chapter B). Moreover, many practical advice and recommendations are presented (preventing issues of DC offsets a high-gain frequency bands, instability compensations, etc.). Also, as a side note a versatile type of electronically controllable bilinear transfer segments, i.e. two-ports allowing an independent electronic control of zero and pole of a transfer function. It is based on a modified current differencing unit (MCDU) as a part of a novel two-path system of the fractional-order proportional-integral or a derivative (FOPI/D) controller [35].

***Objective 2*: Proposal of novel active synthetic impedance (inductor) using current gain adjustment for simple electronic (voltage) tuning of equivalent inductance as well as losses of the synthetic inductor. This feature is not typically solved in similar state-of-the-art solutions (or standard operation amplifier-based solutions).**

This objective presents design and study of difference between integer and fractional-order impedance (synthetic inductor) allowing impedance magnitude adjustment (inductance value adjustment). The adjustment of equivalent inductance is provided by a single current gain (controlled by DC voltage) and an adjustment (or minimization) of serial losses by the second adjustable current gain parameter. Therefore, presented topology fulfills the intended target of this objective regarding standard solutions in literature.

The objective was also addressed and actualized throughout the entire thesis. It is crucial to alter parameters (ideally DC voltage) of the final network structure without having to modify the internal configuration of the circuit. Chapter D presents paper that addresses this issue. It employs widely used and electronically controllable current conveyors, integrating CPE elements in the process for integrating more electronic controllability of the magnitude of input impedance via DC voltage V_{SET_B} parameter Chapter D, [36].

***Objective 3*: The last objective targets the implementation of fractional-order behavior in the design of special resonator with feature of magnitude response reconfigurability. This feature was not tested in a selective transfer response generation, but in several fractional-order reconfigurable two-ports (filters).**

This field of study is not so well described or published in literature. The proposed solution introduces distinctive transfer responses, not present in conventional models, that have significant potential in various applications, such as adaptive frequency equalizers and random distortion level control. For instance, the fractional-order resonator implementation may be used in the phase/frequency detection or in achieving synchronization between two signals of the same frequency and phase. These topics are thoroughly discussed in Chapter E.

4 Concluding Discussion

This doctoral thesis has firstly undertaken a comprehensive initial analysis for electronical application of fractional calculus and its theoretical foundations, tracing its developmental trajectory, and highlighting its expanding integration into diverse scientific and engineering disciplines such as novel the topology of the $PI^{\alpha}D^{\beta}$ regulator, which can be seen in Chapter A: *Practical Design of RC Approximants of Constant Phase Elements and Their Implementation in Fractional-Order PID Regulators Using CMOS Voltage Differencing Current Conveyors*. This marks the author's initial impact journal publication in their doctoral studies, thus signifying its importance. It addresses the complexities and methodologies for the design and application of $PI^{\alpha}D^{\beta}$ regulators, topology utilizes fabricated complementary metal–oxide–semiconductor (CMOS) voltage differencing current conveyors (VDCC), and the detailed design of the CPE element. Furthermore, it provides a critical in-depth analysis of the current research of the state, and a comparison of selected contemporary works up to the date of this publication Chapter A. Work continues with deeper understanding of the analysis of specific types of transfer functions obtained by the summing operation of integer-order and fractional-order two-port responses. Various operations provided by fractional-order, two-terminal devices utilizing those kinds of electronically reconfigurable elements and their Mathcad simulation could be seen in Chapter B: *Integer-and Fractional-Order Integral and Derivative Two-Port Summations: Practical Design Considerations*. Following by the next group of articles with main authorship comprises of conference paper, marking contributions to the field of higher order differentiator synthesis. The first that could be seen in Chapter C: *Higher Order Differentiator Block for Synthesis of Controllable Frequency Dependent Elements*, delves into the development of a sophisticated framework for creating elements that exhibit frequency-dependent behaviors, structure of generally nth-order differentiator transfer block serving for purpose of integer order or fractional order immittance synthesis.

The second key insight of this dissertation is realization of reconfigurable impedance converter in Chapter D: *Reconfigurable Impedance Converter for Synthesis of Integer and Fractional-Order Synthetic Elements*, introduces an innovative approach to designing a clear and practical perspective on a circuit design utilizing electronically controllable current conveyors (ECCII), wide-band operational transconductance amplifiers (OTA), and differential difference amplifiers implemented as voltage buffers, alongside four-quadrant current-mode multiplier Chapter D.

Following traditional integer-order mathematical models often fall short in accurately describing the behavior of complex systems. The introduction of the fractional calculus into these models introduces a level of sophistication and accuracy previously unattainable, allowing for a more tunable utilization. Such a publication could be seen in Chapter E: *Electronically Reconfigurable and Tunable Fractional-Order Filter Using Resonator Concept and Feedforward Path for Low-Frequency Tone Signalization*. The reader is introduced to a comprehensive comparison of filter principles featuring transfer response reconfiguration capabilities within this work. Highlighting the contributions of this research, a novel solution for a special fractional-order filter is proposed. This includes illustrations of examples

demonstrating ideal system behavior alongside with results from the practical testing, allowing for a direct comparison. The detailed analysis not only showcases the theoretical design but also validates the proposed model through empirical and experimental evidence. Presented discussions have highlighted not only the theoretical advancements in the field but also the practical implementations and the potential for any future innovations Chapter E.

4.1 Future Research Possibilities

The exploration of fractional calculus within this thesis opens a multitude of avenues for future research, particularly in enhancing the design and application of advanced circuit elements. Building on the foundational work presented, further investigation could delve into optimizing the ECCII, OTA, and differential difference amplifier (DDA) configurations for even more possibilities of reconfigurability with simple DC control as well as broader bandwidths and higher efficiency. Additionally, the integration of all above mentioned structures (CPEs, immittances, fractional-order resonators, etc.) on CMOS integrated chip technology in novel fractional-order systems to unlock new capabilities in signal processing, control systems, minimalization of parasitic effects in real behavior and beyond. Experimental verification of these advanced designs remains a critical step, offering valuable insights into their practical applications and limitations. It would be advisable to expand the frequency spectrum usability of CPE elements to the widest possible band (GHz). Moreover, the development of comprehensive models that bridge theoretical predictions with real-world performance will be crucial in advancing the field. As computational resources and algorithms continue to evolve, so there will be the potential for simulating increasingly complex systems, enabling groundbreaking innovations in fractional calculus applications.

4.2 Main Body of the Thesis

Following the main body of the dissertation (excluding the bibliography) the subsequent section titled "Publications and Research" along with "A Publication Summary Related to Objectives of Work" compiles all publications related to the author's Objectives of Work. The following chapter "Timeline and Summary of Other Publications with an Author's Contribution" consists of other papers that are not primarily connected to Objectives of Work (papers are mostly second authorship). This segment offers a clear and organized timeline of research outputs, such as journal articles, conference papers, and main or second authorship. Each entry is accompanied by symbolic representations to easily distinguish the type of publication and authorship status.

Furthermore, this part methodically lists all publications directly related to Objectives of Work from Chapter A to Chapter E for the first part of Publication and Research. And Chapter F to Chapter H for the second part. Chapters F to H do not directly solve any objectives related to the dissertation but they are the main part of the author's study (second authorship) and thus significantly adding to the author's research growth. All papers detail instances in the raw format as they appeared in their respective publications. Preceding each article with a "Bibliographic citation", "Author's Contribution" to clarify the extent of involvement.

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PUBLICATIONS AND RESEARCH

A Publication Summary Related to Objectives of Work

Timeline and Summary of Other Publications with an Author's Contribution

A Publication Summary Related to Objectives of Work

Objective 1

Practical Design of RC Approximants of Constant Phase Elements and Their Implementation in Fractional-Order PID Regulators Using CMOS Voltage Differencing Current Conveyors

(impact factor: 2.715, Scopus, 2023)

This paper brings a practical and straightforward view on the design of circuit elements described by fractional-order dynamics known as the constant phase element and their implementation in a novel structure of a PIαDβ (or PIλDμ in some literature) regulator based on fabricated CMOS voltage differencing current conveyors. Step-by-step design of the CPE as well as the PIαDβ regulator is supported by experiments with active devices fabricated using the C07 I2T100 0.7 μm CMOS process (ON Semiconductor). Presented in the journal Circuits, Systems, and Signal Processing (CSSP). Objective 1

Authors: Domanský, O.; Šotner, R.; Langhammer, L.; Jeřábek, J.; Psychalinos, C.; Tsirimokou, G.

Objective 1

Integer-and Fractional-Order Integral and Derivative Two-Port Summations: Practical Design Considerations

(impact factor: 3.143, Scopus, 2023)

This work targets the design and analysis of specific types of transfer functions obtained by the summing operation of integer-order and fractional-order two-port responses. Various operations provided by fractional-order. However, this topic needs to be further studied, and the topologies need to be analyzed in order to extend the state of the art. The studied topology utilizes the passive solution of a constant-phase element. This work was published in journal Applied Sciences by MDPI. Objective 1

Authors: Šotner, R.; Domanský, O.; Jeřábek, J.; Herencsár, N.; Petržela, J.; Andriukaitis, D.

Objective 1

Higher Order Differentiator Block for Synthesis of Controllable Frequency Dependent Elements

This paper presents a structure of generally nth-order differentiator transfer block serving for purpose of integer order or fractional order immittance synthesis. Presentation was commenced during the proceedings at 27th International Conference Radioelektronika 2017. Objective 1

Authors: Domanský, O.; Šotner, R.; Petržela, J.; Langhammer, L.; Dostál, T.

Objective 2

Reconfigurable Impedance Converter for Synthesis of Integer and Fractional-Order Synthetic Elements

This paper introduces a practical and straightforward view on the design of a circuit based on electronically controllable current conveyors, wide-band operational transconductance amplifier, voltage buffer and four quadrant current-mode multiplier. All these elements are implemented for the possibility of multiple electronical tunability of the resulting specific reconfigurable impedance converter of the integer-order as well as the fractional-order. Novelty of this paper was presented at Proceedings of IEEE 2018 41st International Conference on Telecommunications and Signal Processing (TSP 2018). Objective 2

Authors: Domanský, O.; Šotner, R.; Langhammer, L.

Objective 3

Electronically Reconfigurable and Tunable Fractional-Order Filter Using Resonator Concept and Feedforward Path for Low-Frequency Tone Signalization

(impact factor: 4.255, Scopus, 2023)

The last work of my study (as well as the paper with the biggest impact factor of this dissertation) is a novel electronically reconfigurable fractional-order filter allowing independent electronic frequency tuning and switchless change of the transfer response by a single parameter between a standard band-pass, inverting all-pass response and a special type band-reject response. The proposed fractional-order filter tunability yields one-decade range approximately between 10 Hz and 100 Hz. Cadence simulations as well as experimental tests using integrated cells of special multipliers fabricated in ON Semiconductor 0.35 µm I3T25 CMOS. This work was published in IEEE Access journal with the open access version. Objective 3

Authors: Domanský, O.; Šotner, R.; Langhammer, L.; Polák, L.

Legend: - journal article; - conference paper

- main authorship; - second author

A Practical Design of RC Approximants of Constant Phase Elements and Their Implementation in Fractional-Order PID Regulators Using CMOS Voltage Differencing Current Conveyors

Objective 1; (impact factor (2022): 2.311)

Outline

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Author's Contribution

Further research of the original master's thesis of the author. The author proposed the concept, co-designed the methodology, performed realization, analysis, validation, and data visualization. Also worked on finalization and the whole manuscript i.e. reviewing,

editing, etc. The Objective 1 of this paper was fulfilled by the novel topology of PID using voltage differencing current conveyors (VDCC) and two CPE devices. The electronic adjustment allows simple time constant control by DC voltages and currents. It is available for implementing special CMOS active devices and circuit topology using only grounded passive elements (including CPEs). This fact is beneficial for possible integration of the complete device.

Author's contribution: 48 % (the main author).

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Practical Design of RC Approximants of Constant Phase Elements and Their Implementation in Fractional-Order PID Regulators Using CMOS Voltage Differencing Current Conveyors

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Abstract

This paper brings a practical and straightforward view on the design of circuit elements described by fractional-order dynamics known as the constant phase element (CPE) and their implementation in a novel structure of a $PI^{\alpha}D^{\beta}$ (or $PI^{\lambda}D^{\mu}$ in some literature) regulator based on fabricated CMOS voltage differencing current conveyors. Comparison of presented topology with known solutions indicates significant improvements regarding overall simplification, simpler electronic controllability of time constants, and having all passive elements in grounded form. Step-by-step design of the CPE as well as the $PI^{\alpha}D^{\beta}$ regulator is supported by experiments with active devices fabricated using the C07 I2T100 0.7 μm CMOS process (ON Semiconductor). Laboratory tests in frequency and time domain confirm the correct operation of the designed application and the accuracy of the derived results in comparison with the theoretical expectations.

Keywords Constant phase element (CPE) · Differentiator · Fractional-order circuit · Integrator · Proportional branch · Proportional integrational and differential controller (PID) · Voltage differencing current conveyor (VDCC)

1 Introduction

In recent years, fractional elements [43] have attracted increasing attention of researchers because of their interesting behavior in both the time and frequency domain. Fractional calculus has been well known in the mathematical domain for decades, but its potential in electronic circuits with lumped parameters has not been fully explored in detail. Practical implementation of these elements (such as two ter-

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minals or one port) in electronic systems delivers new applications in the field of signal filtering and generation of signals (both harmonic and non-harmonic).

1.1 Constant Phase Element (CPE)

A fractional-order element, known also as constant phase element (CPE), is characterized by a constant phase shift, in the interval between 0° and ±90°, between response (voltage or current) and excitation (voltage or current) in the entire frequency band (ideally from zero to infinity) [43]. The main difficulty for practical application of CPEs is their commercial unavailability. Several solutions of CPEs based on electrochemical [1, 2, 7, 18, 21] organic material [20, 40], polymer composites [11], and thick film layers of resistive, dielectric and insulating materials on silicon [42] have been introduced in recent years. Therefore, these devices are commonly approximated by standard electronic components in passive [24, 31, 43] or active (see for example [37, 41] and references cited therein) implementation. Various active elements [6] can be used in active solutions if limited frequency bandwidth is sufficient.

The simplest ways of CPE imitation are based on suitably arranged infinite series of linear resistors and capacitors in serial/parallel combinations [43]. In practice, there are several methods leading to the design of specific approximations. These so-called ladder structures are very beneficial for purposes of approximation of fractional elements. Their utilization can lead to the creation of two-terminal devices having symbolical mathematical character of immittance function of the Laplace operator $s^{\pm\alpha}$, where $0<|\alpha|<1$. There are several special cases, e.g., when $\alpha=0.5$, where CPE behaves as a so-called half capacitor [26, 37]. Note that in order to allow real implementation, all these known approximations work with limited and finite number of resistances and capacitances in resulting ladder structures. Therefore, the bandwidth of approximation is also restricted. Also, the phase response fluctuates around a mean value with a certain phase ripple being acceptable for particular applications.

The most important guidelines for initial studies in this area, from a mathematical point of view, have been presented in [22, 26, 32, 33]. In the last few years, many papers have significantly contributed to the improvement in this field [31]. Later, methods for widening the frequency range of constant phase shift have been introduced (see for example, [43, 44]). The work in [43] is based on the geometric series of elements, setting initial parameters like phase change, phase ripple, and number of segments. Note that this method is very important for designing the CPEs in this paper. However, this approach is valid up to several MHz. Therefore, CPEs became popular and their behavior and parameters are the main focus of recent studies; for example, influence of roughness [2], capacitance [9] or for filtering [25, 34, 36] of signals with increasing [27] or decreasing [26] phase shift.

1.2 State of the Art of Fractional-Order Passive Elements and PI$^{\alpha}$D$^{\beta}$ Regulator Designs

The contribution of this paper is the employment of already designed CPEs into proportional, integrational and differential controllers (PIDs). The PIDs serve for regulating

the input signal into desirable controlled output. Initial studies of this topic and resulting advantages/features were introduced in [4, 32]. Those papers are mainly theoretical and use general operational amplifier (opamp) structures with presented results concerning stability, gain and phase responses. Integer-order PID regulators are significant in the field of applications in automation and regulation theory [4] and practice [5]. However, the fractional-order solutions [8, 12, 15, 16, 30, 43] can be even more beneficial in these applications. In general, the main difference between integer-order and fractional-order PID is that the fractional-order solution offers two extra degrees of freedom, making the tuning of such controllers easier than that of the conventional (i.e., integer order) counterparts. The first fractional $PI^{\alpha}D^{\beta}$ (also known as $PI^{\lambda}D^{\mu}$) controller was mentioned in [30] where two approaches of fractional calculus are described (the Lenikov-Riemann–Liouville definition and the Caputo definition).

Table 1 shows a list of relevant previously reported PID solutions and provides a simple comparison of their key features. Based on Table 1, we can see that PID concepts suffer from several drawbacks: (a) high number of active elements [13, 14, 23, 35], (b) high number of passive elements [19, 23, 43], (c) impossible electronic tunability [3, 13, 19, 43], (d) floating passive elements [19, 23, 28, 43], and (e) lack of simple (electronical) change of polarity of transfer response (i.e., PID branch transfer) [3, 13, 14, 19, 28, 29, 35, 43]. We are comparing both integer-order and fractional-order solutions in Table 1 because our solution can be easily implemented in both these cases as well as integer-order PID solutions in Table 1 can be easily modified to fractional-order PID regulators when standard capacitors are replaced by fractional-order CPEs and vice versa. Therefore, important novelty of our contribution consists in circuit topology of PID regulator and consequent advantages.

The last noted issue (e) is very important and by fixing it, we may bring some new feature(s) in the area of PID regulators. Direct electronic modification of polarity of integrating or differentiating branch does not require changing PID topology. It is actually a very interesting feature increasing the universality of the proposed PID topology in real applications in regulating/controlling systems for instance. The proposed solution presented in this paper solves each of the discussed issues of previously reported circuits simultaneously. To the best of the author's knowledge, these features have not been reported yet. We can claim that the main novelty of the proposed design consists in its simplicity of topology (as compared with current state of the art) and the possibility of electronic control of parameters of the PID regulator due to the control of the transconductance or the resistance of current input terminal of each VDCC element. Those parameters serve for changing the polarities of transfer in each branch and tuning of time constants as well as changing the gain of a proportional branch. These features are not available simultaneously in previous designs presented in the literature.

The paper is organized as follows: Sect. 2 deals with defining the ideal CPE element and the necessary steps leading to selecting appropriate values of passive components of real CPE created by a selected RC ladder structure. This part explains in detail the calculation, design procedure, and final optimization in order to use a combination of resistors and capacitors of the common fabrication series E24. This Section also shows the effect of tolerances of RC elements on the Monte Carlo analysis. Section 3 continues with the designed CPE and its application into a new solution of a $PI^{\alpha}D^{\beta}$

Table 1 Comparison of PID conceptions based of different active elements

	No. of passive elements	No. of active elements	Type of active elements	Technology	All resistors grounded	All capacitors grounded	Type of control
[43]	8	4	Opamp	Bipolar (commercial IC)	No	No	Passive only (value of C)
[43]	8	4	Opamp	Bipolar (commercial IC)	No	No	passive only (value of R)
[14]	3	8	OTA	CMOS (AMS 0.8 μm)	Yes	Yes	g_m
[29]	3	3–4	DVCC, OTA	N/A	Yes	Yes	R_X, g_m
[28]	3	4	OTA	N/A	Yes	No	g_m
[35]	2	6	OTA	CMOS (TSMC 0.18 μm)	N/A	Yes	g_m
[3]	5	2	CCII	CMOS (TSMC 0.35 μm)	Yes	Yes	Passive only (value of R and C)
[13]	4	8	OTA	Bipolar (AT&T)	Yes	Yes	passive value of R, C and g_m
[19]	10	4	CDBA	CMOS (N/A)	No	No	Passive only (value of R and C)
[23]	63 (60)	11 (12)	Opamp +FPAA[d]	Bipolar (commercial N/A)	No	No	CAB (passive R, C)/FPAA[d]
[10]	10	26	OTA	CMOS (AMS 0.35 μm)	N/A	Yes	g_m
	Proposed						
This work	4	4	VDCC	CMOS ON (0.7 μm)	Yes	Yes	g_m

Table 1 continued

	Electronic control of branch polarity	Type of verification	No. of approx. decades (bandwidth)	Fractional order	Power consumption [mW]	Area (large—commercial opamps/small-fully integrated)	Cost (high—integrated circuit/low—opamps)
[43]	No	Simulated	N/A[a]	No	N/A	Large	Low
[43]	No	Simulated	N/A[a]	Yes	N/A	Large	Low
[14]	No	Simulated	N/A	No	N/A	Large	Low
[29]	No	Simulated	7[b]	Yes	N/A	Large	Low
[28]	No	Simulated	3	Yes	N/A	Large	Low
[35]	No	Simulated	6[c]	No	1.44	N/A	N/A
[3]	No	Simulated	N/A	No	N/A	Large	Low
[13]	No	Simulated	N/A	No	N/A	Large	Low
[19]	No	Simulated	N/A	No	N/A	Large	Low
[23]	No	Simulated/measured	1	Yes	N/A	Large	Low
[10]	No	Simulated	4	Yes	N/A	Small	High
	Proposed						
This work	Yes	Simulated/measured	4	Yes	120	Large	High

Opamp (opamp), operational amplifier; OTA, operational transconductance amplifier; DVCC, differential voltage current conveyor; VDCC, voltage differencing current conveyor; CCII, current conveyor (second generation); CDBA, current differencing buffered amplifier; CMOS, complementary metal–oxide–semiconductor; CAB, configurable analog blocks; FPAA, field-programmable analog array

[a]Study focuses on theory of general design of CPE

[b]CPE used in [29] was theoretically designed for operation up to 1 GHz but real features of elements (dispersion of small values of capacity) limit usability up to several MHz in practice

[c]Magnitude response designed for range 40 Hz–40 MHz (6 decades) but higher corner significantly deviates from ideal trace above 10 MHz

[d]Configurable analog blocks (CAB) based on opamps and field-programmable analog array (FPAA) used together

regulator based on voltage differencing current conveyor (VDCC) active elements. Various experimental benchmarks are also presented. At the end of Sect. 4, the main benefits of the experimentally tested PID are summarized as well as the overall results of the proposed structure.

2 Practical Design of Passive CPE

Dynamics of the non-integer order passive two-terminal element can be characterized with its impedance and admittance. Such an element can be described by the Laplace transformation as admittance:

$$Y_\alpha(s) = \frac{I_{\text{in}}(s)}{V_{\text{in}}(s)} = Y_o \cdot s^\alpha, \tag{1}$$

where the order of CPE (α) can be within the range of $-1<\alpha<1$. The substitution $s = j\omega$ results in complex frequency response of CPE:

$$\hat{Y}_\alpha(j\omega) = Y_o \cdot (j\omega)^\alpha = Y_o \cdot \omega^\alpha e^{j\varphi} = Y_o \cdot \omega^\alpha(\cos\varphi + \mathrm{j} \cdot \sin\varphi), \tag{2}$$

where φ represents the phase shift given by the formula: $\varphi = \alpha\frac{\pi}{2}$ [rad] or $\varphi = 90\alpha$ [degree or °]. The exponent α characterizes the final admittance, and it corresponds to a fractional capacitor ($0 < \alpha < 1$) or to a fractional inductor ($-1 < \alpha < 0$). In the case that $\alpha = 0$, a real resistance is obtained. The Laplace transform can be used in order to convert this function into a rational function with the following pole-zero form:

$$Y(s) = \frac{\sum_{i=1}^{m-1} A_i s^i}{\sum_{k=1}^{m} B_k s^k} = Y_o \frac{\prod_{i=1}^{m-1}(s - \omega_{zm})}{\prod_{k=1}^{m}(s - \omega_{pm})}. \tag{3}$$

The roots and coefficients of (3) determine the phase change φ and the ripple $\triangle\ \varphi$ as will be explained in the following section. Symbols ω_{zm} and ω_{pm} represent the zeros and poles. When the number of sections (i.e., the number of serial RC, RL branches in parallel—between two nodes or serial chain of parallel RC, RL sections) is infinite, phase ripple should be almost equal to zero in the working bandwidth and magnitude response of admittance plot should be linearly increasing/decreasing with $20 \cdot \alpha$ dB per decade.

2.1 Available Passive Structures Suitable for CPE Synthesis

As already mentioned above, there are several ways on how to create a CPE element (which guarantees constant phase shift in a predetermined frequency band). The most promising and useful structure approximating CPE seems to be resistor–capacitor topology (RC [43]). The second possibility is resistor–inductor topology [25]). Because of its complexity and requirement of high accuracy of inductor values, this structure is not used as frequently as the RC combination. If RL topologies are not

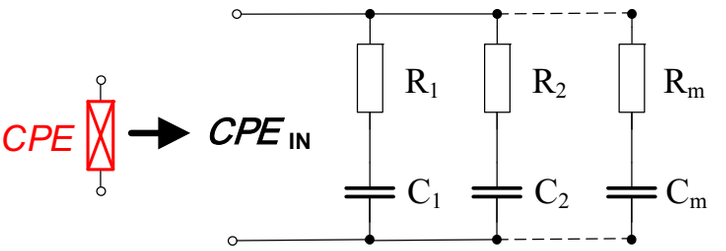

Fig. 1 First possible approximation of CPE by parallel combination (branches) of serial RC segments

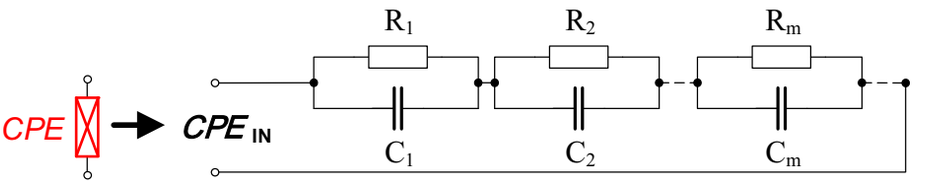

Fig. 2 Second possible approximation of CPE by serial combination (serial chain) of parallel RC segments

used, many practical problems appearing in systems using metal coils (weight, size, mechanical fixation, electromagnetic field radiation, etc.) are avoided.

The following solutions of CPE can be recognized as more beneficial than the previously mentioned RL because no inductors are required. A particular solution can be created by serial RC segments in parallel branches as shown in Fig. 1. This topology has the following symbolical form of admittance:

$$Y(s) = \sum_{i=1}^{m} \frac{sC_i}{sC_iR_i + 1}, \tag{4}$$

where m is the number of branches.

The second possible RC topology (Fig. 2) has the following overall impedance expression:

$$Z(s) = \sum_{i=1}^{m} \frac{R_i}{sC_iR_i + 1}. \tag{5}$$

Moreover, frequency features (especially bandwidth of approximation) of above-noted simple circuits can be significantly improved when so-called correction elements [43] are added (Fig. 3). Figure 4 shows exemplary phase response of CPE designed by parallel combination (Fig. 1) compared with phase response of the same CPE designed also with so-called correction elements (Fig. 3). Additional correction elements help to significantly improve response in low- and high-frequency corners. Therefore, the frequency range of CPE is significantly extended (Fig. 4, red trace). These additional elements create additional zeros in the overall admittance function that intentionally gets shifted to low frequencies for resistance R_p and to higher frequencies for C_p. Correction elements are represented by single capacitance C_p and single resistance R_p in CPE topology shown in Fig. 3. Corrected input admittance of the CPE can be expressed as:

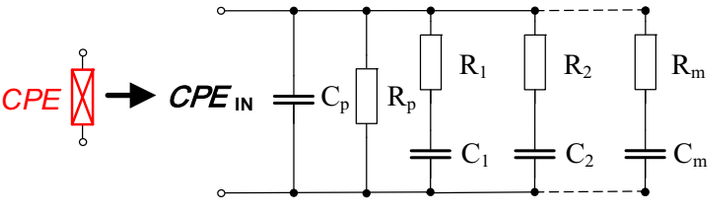

Fig. 3 First possible approximation of CPE structure with correction elements (C_p and R_p)

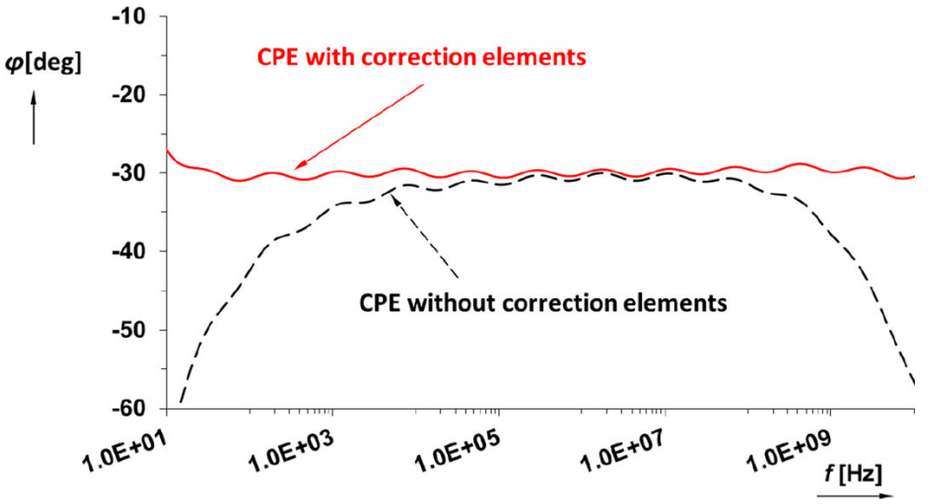

Fig. 4 Ideal phase responses of CPE with (red curve) and without (black dashed trace) correction elements (Color figure online)

$$Y(s) = sC_p + \frac{1}{R_p} + \sum_{i=1}^{m} \frac{sC_i}{sC_i R_i + 1}. \tag{6}$$

Note that simulation results were yielded for particular values of CPE30 from Table 3 (presented later).

2.2 Design Example of Passive CPE

Mathematical background provides several ways [12, 16, 24, 25, 31, 36, 43] for approximating CPEs with desired bandwidth and phase ripple. These approximations lead to a specific distribution of zeros and poles (roots of polynomial expressions) of previously noted passive RL and RC sections [43] or also other passive [26] or active solutions [14]. The selected type of approximation and calculation algorithm is defined and further explained in [43]. Our example shows the design of CPE based on RC topology from Fig. 3.

The first step of our design consists in specifying the performance of the required immittance function. The papers [26, 31, 43] show some generally defined and commonly used values of recommended and achievable phase ripples: $\triangle\ \varphi = 0.05; 0.1; 0.2; 0.5; 1; 2; 5$ degrees. The price that comes with the phase ripple is that if the lower values of phase ripple are needed the more accurate values (lowest tolerances possible) of passive elements are required (for example with $\triangle\ \varphi = 0.05$ tolerances of passive RC elements should not be more than 1% otherwise the phase ripple tolerance will not be fulfilled). CPEs with phase ripple $\triangle\ \varphi > 5$ degrees are

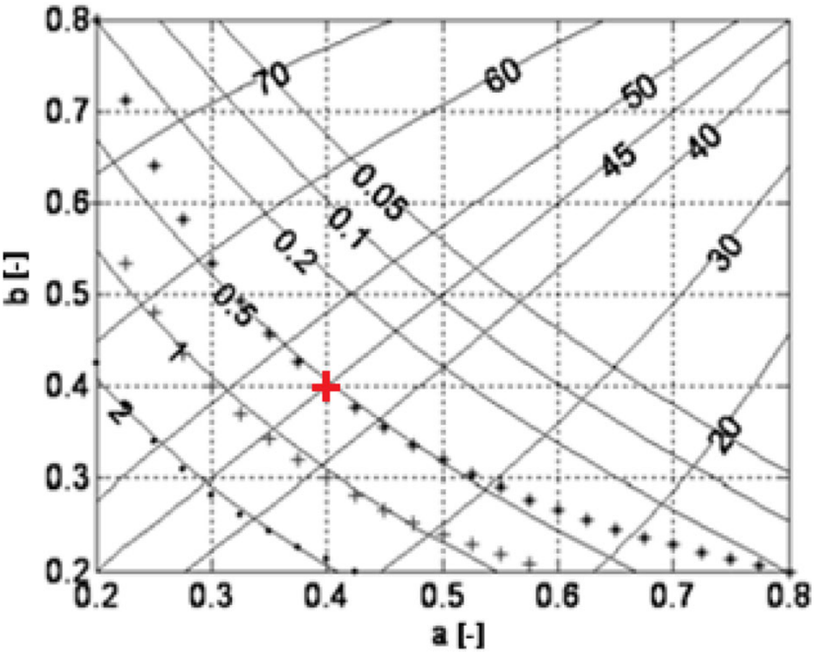

Fig. 5 Nomogram for selection (red cross) of parameters a and b [43] for particular CPE realization (Color figure online)

not suitable for design due to very large phase fluctuation in the operational band of CPE. So, the main reason still consists in selecting components from fabrication series, in fabrication tolerances and also in parasitic effects of real passive components. Presented values of phase ripple represent theoretical values, and therefore, the real ripple will always be higher than ideal expectations. Therefore, the best design option in practice seems to be selecting $\triangle\ \varphi = 0.5$ or 1 degrees in order to keep real phase ripple below 5 degrees. It is also important to note that phase shift φ can be selected in the ideal range from 0° to 90°.

Another parameter influencing the achieved frequency range is the number of branches m (the number of parallel RC segments), where $m \to \infty$ theoretically; however, in practice $m \leq 15$. This parameter affects the operating frequency range. Higher m means wider bandwidth of validity of approximation. Unfortunately, higher m leads to significantly increased complexity of the CPE and also to non-practical values of passive elements (resistances and capacitances). The next design step supposes appropriate selection of input resistance (R_{initial}), capacitance (C_{initial}) (which are the initial parameters, along with $\triangle\ \varphi$ and m, designed to be able to manipulate the final set of values of R_k and C_k and they are further described in the text) and parameter D (modulus). Modulus D is equal to the magnitude value at frequency $\omega = 1$ (normalized). The following parameters define lower (ω_l) and upper (ω_u) limits of frequency range of the final CPE:

$$\omega_l \cong \frac{1}{\tau}, \quad \omega_u \cong \frac{1}{\tau \cdot (ab)^m}, \tag{7}$$

where a and b are non-dimensional empirical values at the axis of nomogram (Fig. 5) [43].

The product of parameters ab determinates theoretically expected values of phase ripple. There are two ways on how to determine values of a and b. The first method is based on nomogram [43] where these parameters can be obtained from the knowledge of expected phase shift φ within the range from 20° to 70° [43] in depending on the desired phase ripple ($\triangle\ \varphi$). For example, if phase change/shift $\varphi = 45°$ with $\triangle\ \varphi = 0.5°$ being required, then the resulting values are: $a = 0.4; b = 0.4 \Rightarrow ab = 0.16$ (Fig. 5).

The second method consists of enumeration of a and b from the following formulas [43]:

$$ab \cong \frac{0.24}{1+\triangle\ \varphi}, \tag{8}$$

$$\alpha = \frac{\varphi}{90}, \tag{9}$$

$$a = 10^{\alpha \cdot \log(ab)}, b = \frac{ab}{a}, \tag{10}$$

It must be worth mentioned that in the last Eq. (10) the final result isn't $b = b$ but only a and the multiplication of ab is known, and therefore, b is needed to be separated.

Knowledge of values of previously discussed parameters allows the calculation of correction elements C_p and R_p:

$$R_p = \frac{R_{\text{initial}}(1-a)}{a}, \tag{11}$$

$$C_p = \frac{C_{\text{initial}} b^m}{1-b}, \tag{12}$$

which are followed by the calculation of subsequent elements in the segments of the serial RC combination:

$$R_k = R_{\text{initial}} a^{k-1} \cdot \frac{D_p}{D}, \quad C_k = C_{\text{initial}} b^{k-1} \cdot \frac{D}{D_p}, \tag{13}$$

where k is the index number of each segment and D_p (normalized to impedance $\omega = 0$) is the modulus that is set by the designer. Now, we have available values of all parts of the overall circuit. Possible admittance of the whole CPE circuit is:

$$Y_{(s)} = \frac{1}{R_P} + sC_p + \sum_{k=1}^{m} \frac{sC_k}{1 + sR_kC_k}. \tag{14}$$

If $s = j\omega$ then ω_τ (angular frequency calculated from R_{initial} and C_{initial}) equals:

$$\omega_\tau = \left(\frac{a}{b}\right)^{\frac{1}{4}} \cdot \frac{1}{R_{\text{initial}} C_{\text{initial}} (ab)^2} \tag{15}$$

Now, modulus D and D/D_p should be calculated. Calculated values of all resistances in the circuit from Fig. 3 are multiplied by the ratio D/D_p, and all capacitances in the circuit will be divided by the ratio D/D_p:

$$D = \frac{\omega_\tau^\alpha}{Y_{(\omega_\tau)}} \rightarrow D_p/D. \tag{16}$$

An example of the calculation is provided for the particular parameters. The number of branches was selected as a compromise between complexity of the design and desired frequency range of the final CPE:

$$m = 14, \quad R_{\text{initial}} = 10\ \text{k}\Omega, \quad C_{\text{initial}} = 1\ \mu\text{F}, \quad \triangle\,\varphi = 0.5^\circ, \quad \varphi = 30^\circ,$$
$$D_p = 10k\,(\text{normalized}),$$

$$ab \cong \frac{0.24}{1+\triangle\,\varphi} = \frac{0.24}{1+0.5} = 0.16, \tag{17}$$

$$\tau = R_{\text{initial}} C_{\text{initial}} = 10 \cdot 10^3 \cdot 1 \cdot 10^{-6} = 0.01\ \text{s}; \quad \omega_l = \frac{1}{\tau} = \frac{1}{0.01} = 100\ \text{Hz}, \tag{18}$$

$$a = 10^{\alpha \cdot \log(ab)} = 10^{\frac{30}{90} \cdot \log(0.16)} = 0.5429, \tag{19}$$

$$b = \frac{ab}{a} = \frac{0.16}{0.5429} = 0.2947, \tag{20}$$

$$R_p = \frac{R_{\text{initial}}(1-a)}{a} = \frac{10 \cdot 10^3 (1-0.5429)}{0.5429} = 8.42 \cdot 10^3 = 8420\ \Omega, \tag{21}$$

$$C_p = \frac{C_{\text{initial}} b^m}{1-b} = \frac{1 \cdot 10^{-6} \cdot 0.2947^{14}}{1-0.2947} = 5.3 \cdot 10^{-13} = 0.53\ \text{pF}, \tag{22}$$

$$\omega_\tau = \left(\frac{a}{b}\right)^{\frac{1}{4}} \cdot \frac{1}{R_{\text{initial}} C_{\text{initial}} (ab)^2} = \left(\frac{0.5429}{0.2947}\right)^{\frac{1}{4}} \cdot \frac{1}{0.01 \cdot 0.16} = 4551\left[\text{rad s}^{-1}\right]. \tag{23}$$

The resulting parameters of admittance are given by:

$$Y(s = j\omega_\tau) = \frac{1}{R_P} + sC_p + \sum_{k=1}^{m} \frac{sC_k}{1 + sR_k C_k} = 0.70\ \text{mS}, \tag{24}$$

$$D = \frac{\omega_\tau^\alpha}{Y_{(\omega_\tau)}} = \frac{4551^{\frac{30}{90}}}{7.0312 \cdot 10^{-4}} = 2.3569 \cdot 10^4 \left[\text{rad s}^{-1}\text{S}^{-1}\right]$$
$$\rightarrow \frac{D_p}{D} = \frac{10 \cdot 10^3}{2.3569 \cdot 10^4} = 0.4243, \tag{25}$$

$$R_1 = R_{\text{initial}} a^{k-1} \cdot \frac{D_p}{D} = 10 \cdot 10^3 \cdot 0.5429^{1-1} \cdot 0.4243 = 4242\ \Omega, \tag{26}$$

$$R_2 = R_{\text{initial}} a^{k-1} \cdot \frac{D_p}{D} = 10 \cdot 10^3 \cdot 0.5429^{2-1} \cdot 0.4243 = 2303\ \Omega, \tag{27}$$

Table 2 Calculated values of CPE for phase change $\varphi = 30°$ (CPE30) without any corrections

$\varphi = 30°$															
	m_k	m_1	m_2	m_3	m_4	m_5	m_6	m_7	m_8	m_9	m_{10}	m_{11}	m_{12}	m_{13}	m_{14}
$R_P(\Omega)$ 3570	$R_k(\Omega)$	4242	2303	1250	679	368	200	108	58	32	17	9	5	2	1
C_P(F) 0.5p	C_k(F)	2.35µ	0.69µ	0.21µ	60n	17n	5.2n	1.5n	0.45n	0.13n	39p	11p	3.4p	0.1p	0.02p

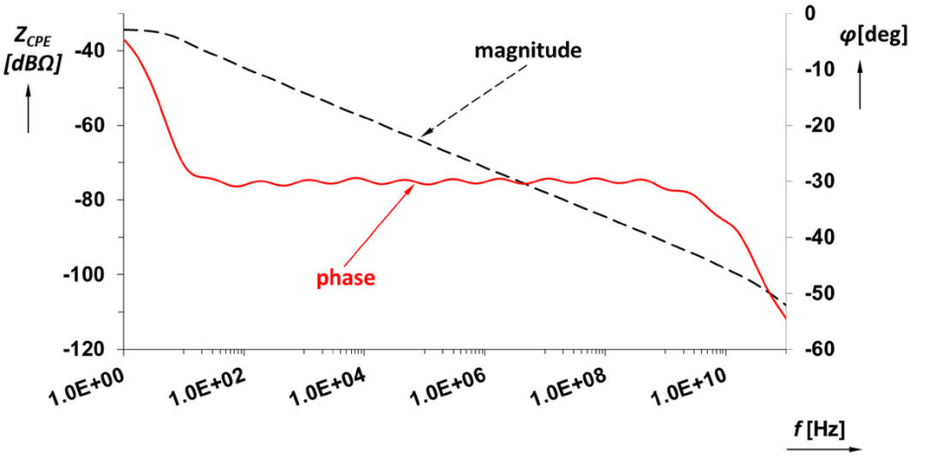

Fig. 6 Simulation results of approximated CPE [for values calculated in (17)–(29)] for phase shift and magnitude

the calculation proceeds similarly for all values of R_k

$$C_1 = C_{\text{initial}} b^{k-1} \cdot \frac{D}{D_p} = 1 \cdot 10^{-6} \cdot 0.2947^{1-1} \cdot 2.3569 = 2.35\ \mu\text{F}, \tag{28}$$

the calculation proceeds similarly for all values of C_k.

$$C_2 = C_{\text{initial}} b^{k-1} \cdot \frac{D}{D_p} = 1 \cdot 10^{-6} \cdot 0.2947^{2-1} \cdot 2.3569 = 0.69\ \mu\text{F}. \tag{29}$$

Calculated values of passive elements of all members of the chain can be seen in Table 2. Realization of such a CPE could be really difficult because values of capacitors and resistors are not in the fabrication series (E24). Small value adjustments, in branches represented by higher value of m, are allowed by changing parameter D_p. For example, an absurd discrete capacitor value $C_{14} = 0.02$ pF is required for $D_p = 10k$ but only for $D_p = 1k$ it is $C_{14} = 2.9$ pF (the location of the root is still sustained).

Simulation results (Fig. 6) confirmed the theoretical design of a CPE for a wide frequency range from 10 Hz up to 200 MHz. Phase ripple is $\triangle\ \varphi < 0.75$ which is a little bit higher than given by theory but still sufficient. The magnitude decreases by 6.5 dB per decade.

However, the designed parameters of this CPE (in this phase of design) need to be optimized. The best compromise between required design accuracy and values of commercially available components selected from a fabrication series must be found.

Table 3 Corrected values of real designed CPE30 for phase change $\varphi = 30°$

$\varphi = 30°$															
	m_k	m_1	m_2	m_3	m_4	m_5	m_6	m_7	m_8	m_9	m_{10}	m_{11}	m_{12}	m_{13}	m_{14}
$R_P(\Omega)$ 3578	$R_k(\Omega)$	4230	2300	1251	680	370	200	110	58	33	18	10	5.1	2.7	1.5
C_P(F) 0.82p	C_k(F)	2.35µ	0.69µ	202n	59.9n	16.8n	5.1n	1.5n	446p	130p	39p	11p	3.3p	0.82p	0.42p

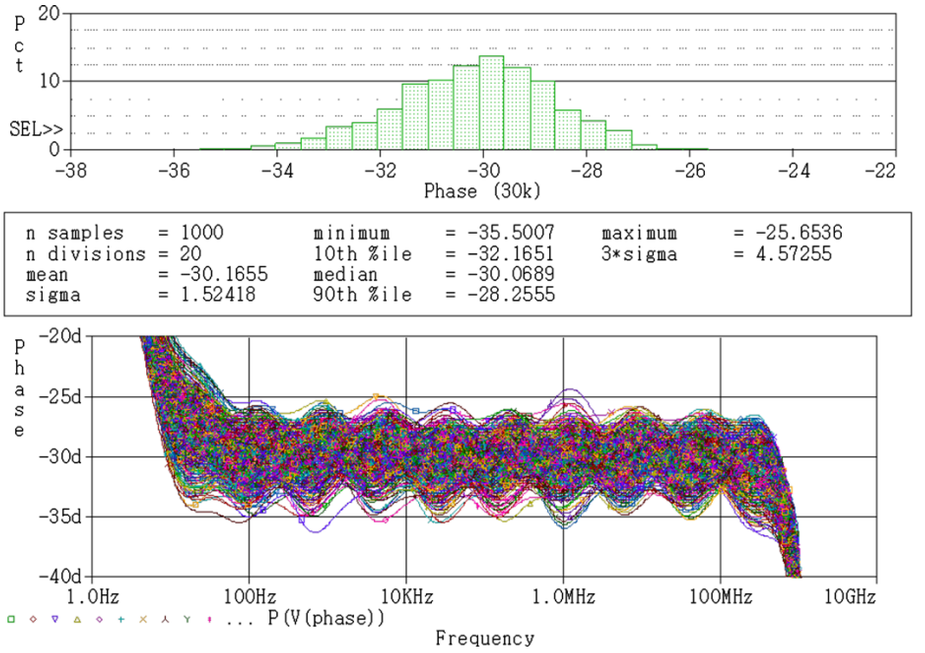

Fig. 7 Histogram and Monte Carlo analysis of CPE with phase change $\varphi = 30°$ for 1000 runs (with tolerances of 20% for capacitors and 5% for resistors)

The CPE and its real design values will be described in the following paragraphs. Difference between approximated and real design can be seen in Tables 2, 3.

The behavior of designed CPE was analyzed by Monte Carlo simulation as well as its histogram (yield for frequency 30 kHz). The analysis was carried out for 1000 runs with 5% tolerance for resistors and 20% tolerance for capacitors.

Figure 7 shows that CPE works well even with expected inaccuracies of the circuit. The main source of deviations, in this synthesis, is capacitor C_p (inaccuracy in C_p yields higher deviations Fig. 7). This capacitor should have as low inaccuracy as possible, especially because of its effect at higher frequencies (more than 10 MHz) where even very small inaccuracy of a value causes a significant change in the circuit bandwidth.

In order to verify the features of approximated CPE by real laboratory experiment, it was necessary to select very accurate values of passive components. Almost all values of the CPE were transformed (assigned) into possible commercially available values of resistors with 1% tolerance and capacitors with 5% tolerance (series E24). Some desired values are a combination of two resistors in series or two capacitors in parallel (for example, $R_1 = 330\ \Omega + 3900\ \Omega = 4230\ \Omega$). The following Table 3 shows their modified values. A universal two-sided board was developed for implementing 14 segments ($m = 14$). Each segment offers the possibility to connect two serial and four

Table 4 Corrected values of real designed CPE22.5 for phase change $\varphi = 22.5°$

$\varphi = 22.5°$															
	m_k	m_1	m_2	m_3	m_4	m_5	m_6	m_7	m_8	m_9	m_{10}	m_{11}	m_{12}	m_{13}	m_{14}
$R_P(\Omega)$ 15k	$R_k(\Omega)$	30.2k	20.2k	13.5k	9k	6k	4k	2.7k	1.8k	1.2k	807	540	361	242	162
C_P(F) 2p	C_k(F)	33µ	1.96µ	870n	389n	174n	78n	35n	16n	7n	3.1n	1.4n	623p	280p	125p

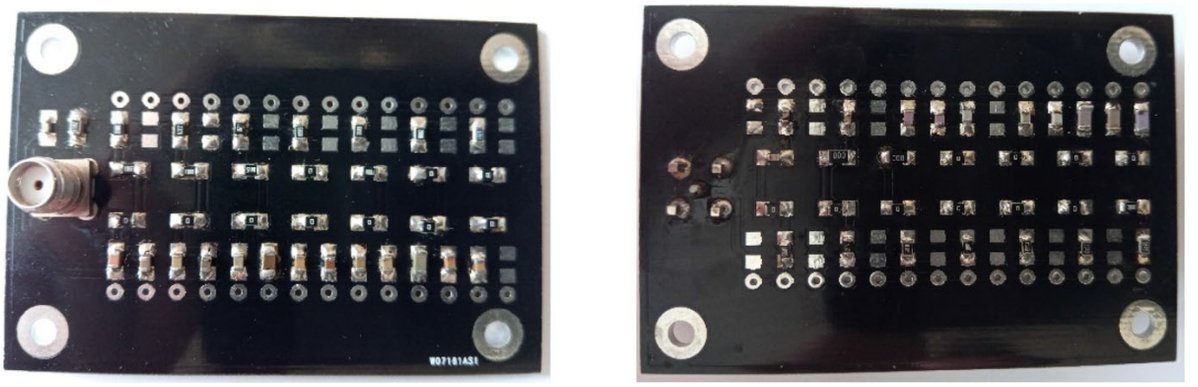

Fig. 8 Photograph of one side of two-sided PCB developed to carry up to 86 (14 branches each consist of 6 passive slots plus 2 slots for correction elements) passive components approximating our CPE (CPE30)

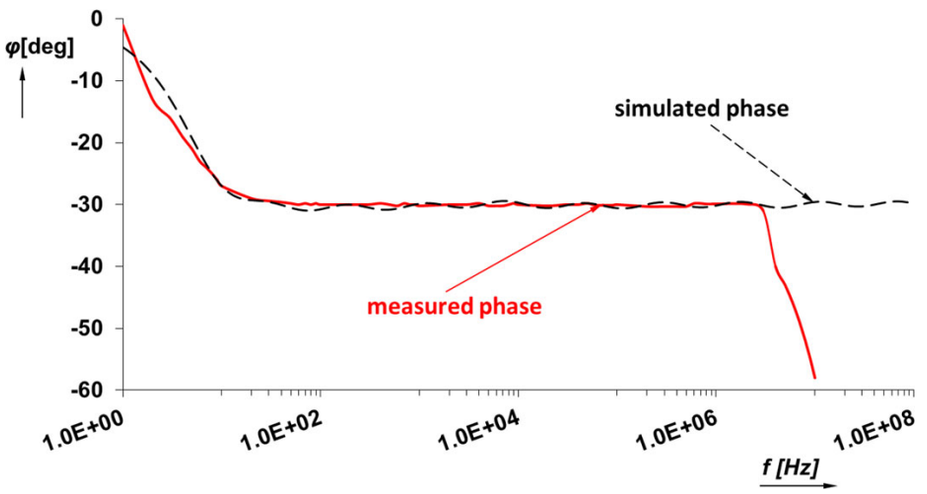

Fig. 9 Comparison of measured and theoretical (simulated) phase response of approximated CPE30

parallel elements simultaneously (occupied with empty footprints ready for additional elements). The same procedure was followed when designing the CPE with phase shift equal to $\varphi = 22.5°$, which is needed for further design steps as described later. Values of passive components of this CPE are described in Table 4. A photograph of the two-sided developed PCB (for $\varphi = 30°$) is shown in Fig. 8.

Exemplary results of real measurements of CPE30 in comparison with theoretical expectations are shown in Fig. 9. Practical usability ends at lower frequency than theory due to real features of the PCB (parasitic capacitances) together with high error of the capacitors at their lowest values.

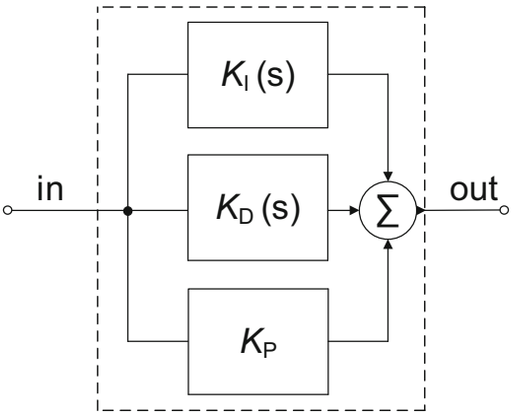

Fig. 10 Block diagram of a general PID controller in variant with SISO topology

3 Special Solution of PI$^{\alpha}$D$^{\beta}$s Based on VDCC Elements

The standard concept of integer-order PID controllers comprises three separate branches, namely the proportional (P), integrational (I), and differential (D) branch. The proportional branch only has a simple task here, and it is the amplification of the input signal without changing its phase. The integrational branch provides decreasing magnitude of transfer response with slope $-20 \cdot \alpha$ dB per decade. Theoretically, the phase shift between the output and input signal should be $-\alpha \cdot 90°$. The differential branch performs an ideal derivative of the input signal with ascending magnitude ($+20 \cdot \beta$ dB per decade) and constant phase shift between the output and input signal equal to $+\beta \cdot 90°$. The symbolical transfer function $K(s)$ of such a circuit is:

$$K(s) = \frac{V_{\text{out}}(s)}{V_{\text{in}}(s)} = K_P + K_I \frac{1}{s^{\alpha}} + K_D s^{\beta}. \tag{30}$$

Possible concepts of PIDs are single-input multiple-output (SIMO) topology (all responses are separated) or to single-input and single-output (SISO) topology, where all responses are combined as is shown in Fig. 10.

3.1 Description of VDCC Element

The proposed solution is based on a structure with four voltage differencing current conveyors (VDCC) as active elements [38, 39]. The VDCC schematic symbol is described in Fig. 11. This device was developed and manufactured as a real CMOS-based device in 0.7 μm I2T100 technology and has been introduced by a behavioral model [17] and developed in [38]. The VDCC device has controllable transconductance ($\pm g_{\text{m}}$), moreover, with a special feature of electronically selectable polarity that is dependent on change of polarity of DC voltage at pin V_{set_gm}. The transfer function between current $\pm I_{z\_TA}$ and input voltages of differential input terminals (p and n) has the form $\pm I_{z\_TA} = \left(V_p - V_n\right) \cdot g_{\text{m}}$. Two outputs ($zp$ and zn) produce positive and negative current copies of I_X ($I_{zp} = I_X$, $I_{zn} = -I_X$). Input resistance of terminal X is adjustable ($R_X \cong 5/\sqrt{I_{set\_Rx}}$ [38]) by the DC control current (Fig. 12). The transfer operation between terminals z_TA and X can be expressed by the following relation: $V_X = V_{z\_TA} + R_X I_X$. The relation between transconductance and DC control voltage is $g_m = 2 \cdot 10^{-3} \cdot V_{set\_gm}$ (graphical representation is shown in Fig. 13). Note that

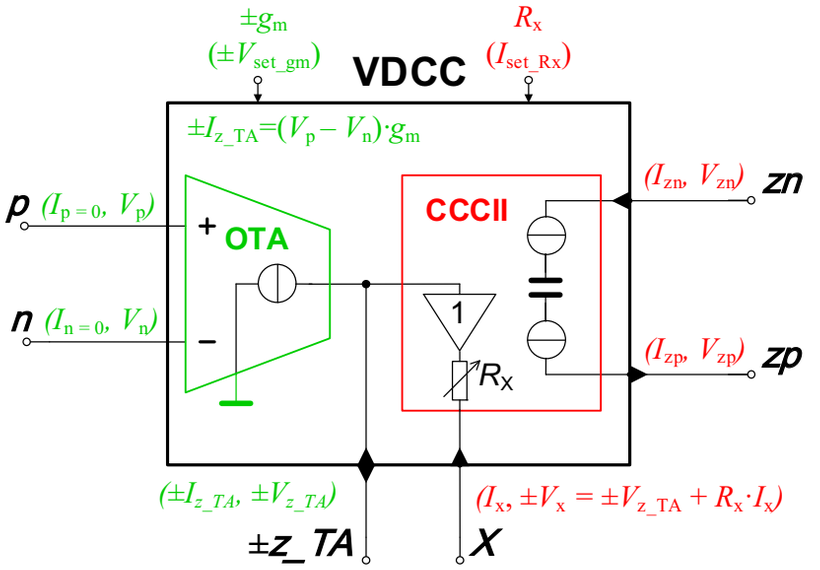

Fig. 11 Internal concept of the VDCC element

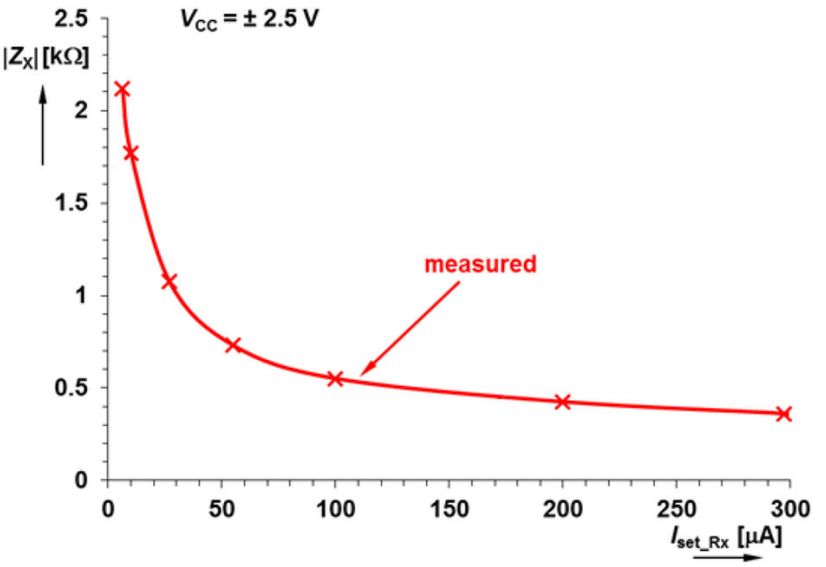

Fig. 12 Measured dependence of internal resistance $R_X(Z_X)$ on bias current I_{set_Rx} of VDCC

other details about VDCC are presented in [17, 38, 39]. Nominal supply voltage of VDCCs in all tests was set to ±2.5 V.

Complete internal CMOS topology of the VDCC element can be seen in Fig. 14. The CMOS topology of VDCC includes four-quadrat voltage mode multiplier followed by the boosting cascoded transconductance section ($V \rightarrow I$ converter). Implementation of the multiplier allows simple achievement of both polarities of the output current from this OTA stage (resulting in $\pm g_m$). The current conveyor part of VDCC has topology modified by special biasing part for cascoded mirrors and two outputs of opposite polarity. The design specifications predetermine OTA part of the VDCC for low-frequency applications (3 dB bandwidth of the relation $I_{\pm z\_TA} = (V_p - V_n) \cdot g_m$) limited up to 2 MHz. The DC performances of the OTA stage are ± 200 mV for voltage input and ± 500 µA for current output. The conveyor stage AC limits can be found around 20 MHz, whereas DC linear range of voltage transfers reaches ± 200 mV and ± 1000 µA for current transfers. The transconductance g_m can be tuned from 0

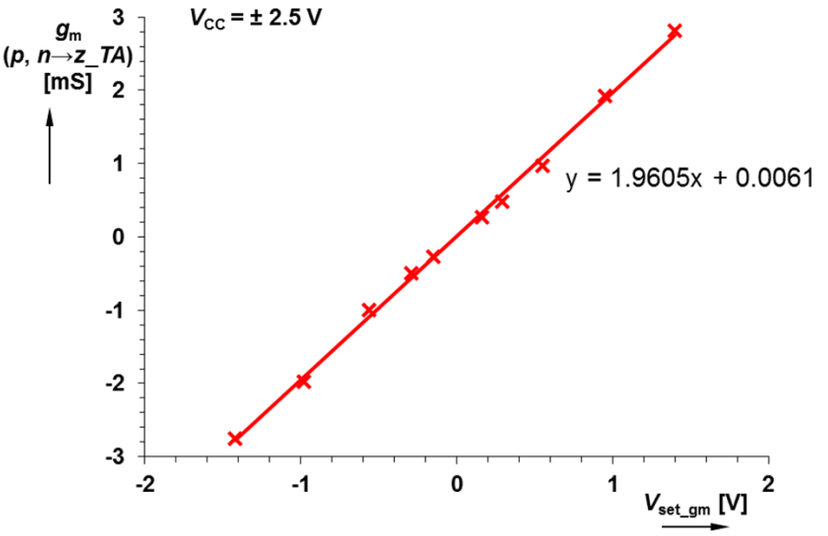

Fig. 13 Measured dependence of transconductance g_m on voltage V_{set_gm} of VDCC

to ± 2.81 mS ($V_{\text{set\_gm}} = 0 \rightarrow \pm 1.4$ V) and resistance R_X adjustable from 2.1 kΩ to 310 Ω ($I_{\text{set\_Rx}} = 6.3\ \mu\text{A} \rightarrow 300\ \mu\text{A}$). For further details, see [38].

3.2 Designed PI$^{\alpha}$D$^{\beta}$ Controller

The final interconnection serving as the PI$^{\alpha}$D$^{\beta}$ regulator is shown in Fig. 15. There are three branches representing the P, I$^{\alpha}$ and D$^{\beta}$ function. Note that the ICs packages (Fig. 27) are implemented in the development board for five ICs (Fig. 27) together with the connected discrete solutions of CPEs (CPE30, CPE22.5) from Fig. 8.

The first of them is based on VDCC$_1$ (I function), the second utilizes VDCC$_2$ and VDCC$_3$ (D function), and the third one requires VDCC$_4$ (P function). Bias current I_{set_Rx1} was set to 100 μA in order to obtain $R_{Xsum1} = R_{Xext1} + R_X = 100\ \Omega + 400\ \Omega = 0.5$ kΩ. The second branch needs two VDCCs for emulating the differentiation operation. The second VDCC$_2$ has feedback loop from pin zn to pin p with X connected to the input node. The CPE$_2$ is connected to the $\pm z\_TA$ pin of VDCC$_2$. VDCC$_3$ serves as a voltage to current converter. All output responses are summarized in the form of current in the output node and transformed to voltage by VDCC$_4$. The terminal X of VDCC$_4$ is used as output of the PID topology (V_{out}) because of its low impedance character in comparison with the high-impedance node where current terminals of all branches are connected together. Parameters of PID can be electronically driven by transconductances $g_{mx}\left(V_{set\_gm}\right)$ of VDCC elements. CPEs designed in the previous section form a significant part of the proposed PID and actually cause the PID to be of fractional order. CPE$_1 = 22.5°$ ($\alpha = 1/4$) was used in the integrational part, and CPE$_2 = 30°$ ($\beta = 1/3$) in the differentiation part of the PID (Fig. 15). For all measurements and simulations, CPE's from Tables 3 and 4 were used.

The overall voltage transfer function (Fig. 16) of this circuit solution (Fig. 15) where s^{α} and s^{β} are orders of the CPEs elements leads to the following:

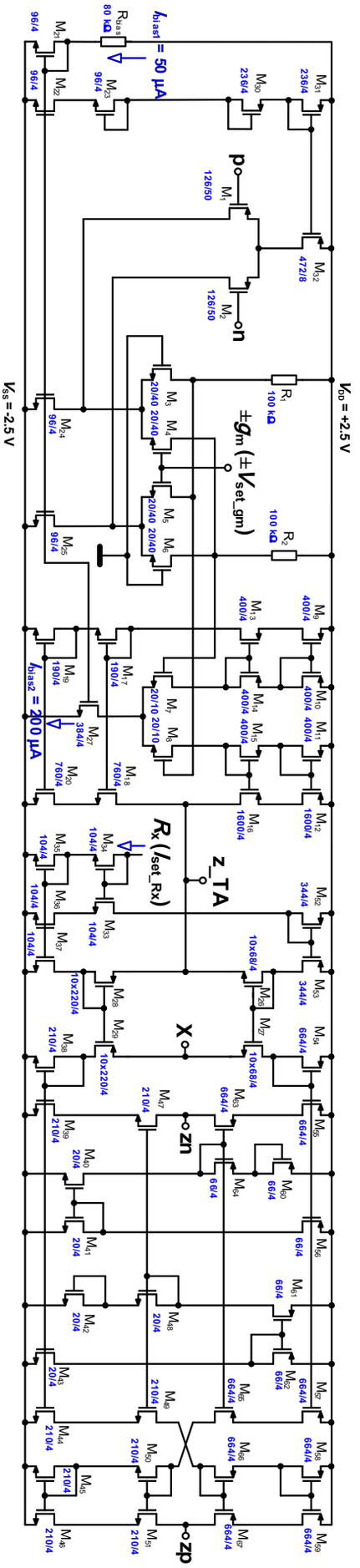

Fig. 14 Complete internal structure of the CMOS VDCC element (Fig. 11)

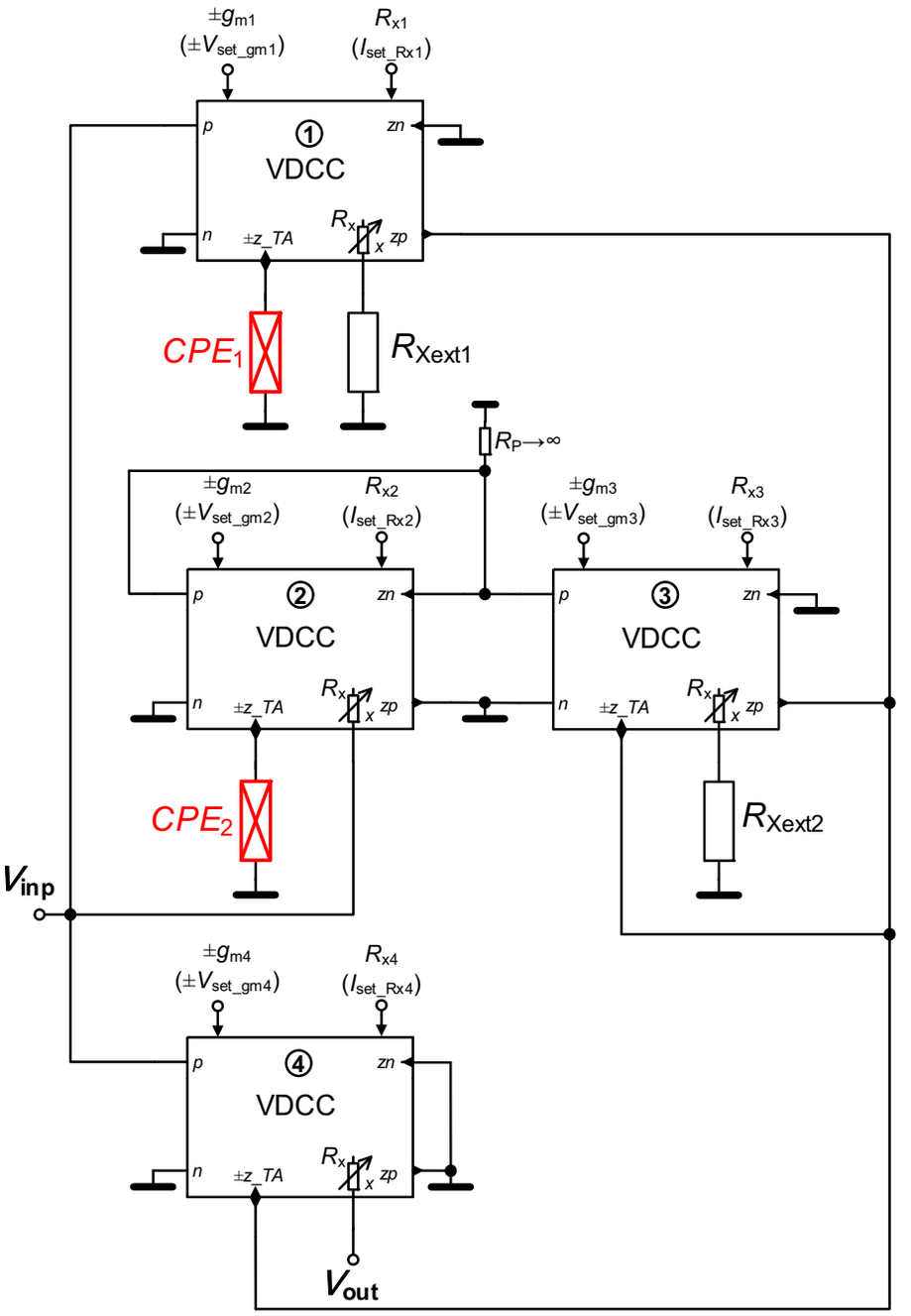

Fig. 15 Designed PID structure employing four VDCC elements fabricated using the 0.7 μm I2T100 CMOS process and two CPE elements

$$\frac{V_{\text{out}}}{V_{\text{in}p}} = \pm\frac{g_{m1}}{s^{\alpha}\cdot C_{CPE1}}\cdot\left[\frac{R_{Xext2}+R_{X3}}{R_{Xext1}+R_{X1}}\right]\pm\frac{s^{\beta}\cdot C_{CPE2}}{g_{m2}} \cdot[g_{m3}\cdot(R_{X3}+R_{Xext2})]\pm g_{m4}\cdot[R_{X3}+R_{Xext2}]\,. \tag{31}$$

When $\left[\frac{R_{Xext2}+R_{X3}}{R_{Xext1}+R_{X1}}\right]=1$ and $g_{m3}\cdot(R_{X3}+R_{Xext2})=1$, (31) simplifies to:

$$\frac{V_{\text{out}}}{V_{\text{in}p}} = \pm\frac{g_{m1}}{s^{\alpha}\cdot C_{\text{CPE1}}}\pm\frac{s^{\beta}\cdot C_{\text{CPE2}}}{g_{m2}}\pm g_{m4}\cdot[R_{X3}+R_{Xext2}]. \tag{32}$$

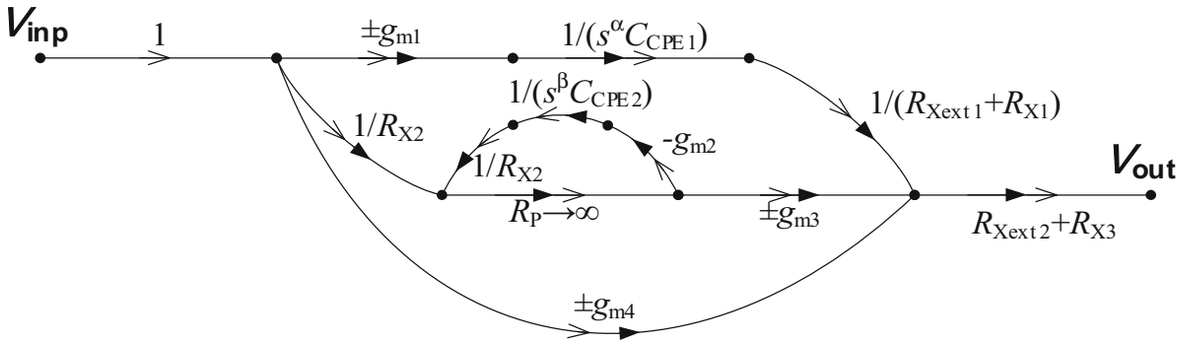

Fig. 16 Signal flow graph of PID structure in Fig. 15

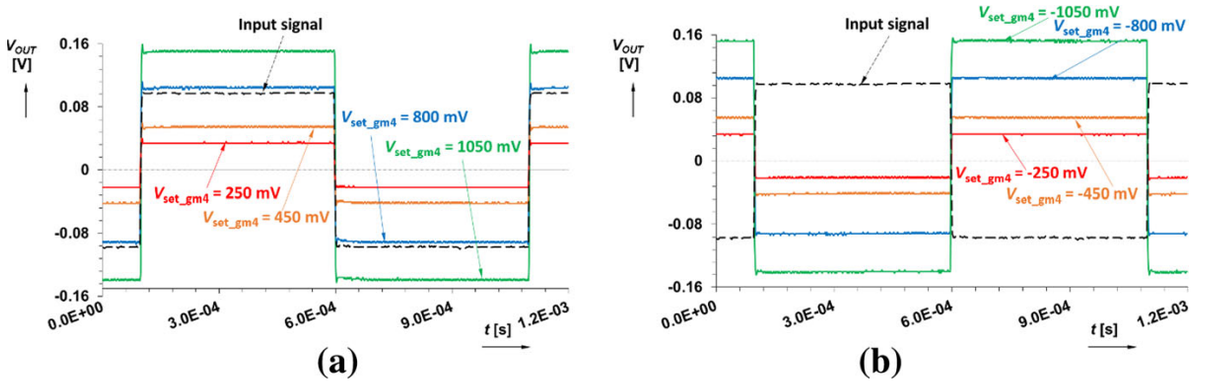

Fig. 17 Transient response of the proportional branch of the designed PID controller: **a** for positive values of V_{set_gm4}, **b** for negative values of V_{set_gm4}

The signal flow graph in Fig. 16 clearly indicates all signal operations in the structure and all three branches of the PID circuit. Note that "parasitic element" $R_{\mathrm{p}} \rightarrow \infty$ in high-impedance node of the differentiator path serves for better regularity of the used method of analysis and precise description of signal operations (transformations between currents and voltages in the loop).

3.3 Measurement Results

Time and frequency measurements of the circuit from Fig. 15 (the test bench and layout of VDCC shown in Figs. 26 and 27) are discussed in the following part. The time domain measurements of the proportional branch for four different settings of V_{set_gm4}($V_{set\_gm4} = \pm 250$ mV $\rightarrow$ $g_{m4} \cong \pm$ 0.5 mS, $V_{set\_gm4} = \pm$ 500 mV $\rightarrow$ $g_{m4} \cong \pm$ 1 mS, $V_{set\_gm4} = \pm$ 800 mV $\rightarrow$ $g_{m4} \cong \pm$ 1.5 mS and $V_{set\_gm4} = \pm 1000$ mV $\rightarrow$ $g_{m4} \cong \pm$ 2 mS) are shown in Fig. 17.

Features of the integrational branch were also tested, and results are shown in Fig. 18. Three values have been set from positive (Fig. 18a) and negative (Fig. 18b) polarity ($V_{set\_gm1} = \pm$ 250 mV $\rightarrow$ $g_{m1} \cong \pm$ 0.5 mS, $V_{set\_gm1} = \pm$ 500 mV $\rightarrow$ $g_{m1} \cong \pm$ 1 mS, $V_{set\_gm1} = \pm$ 1000 mV $\rightarrow$ $g_{m1} \cong \pm$ 2 mS).

In the case of the differential branch, the same set of values for V_{set} was tested, only V_{set_gm1} was replaced by V_{set_gm2}. Results for positive and for negative polarities are shown in Fig. 19a and b, respectively.

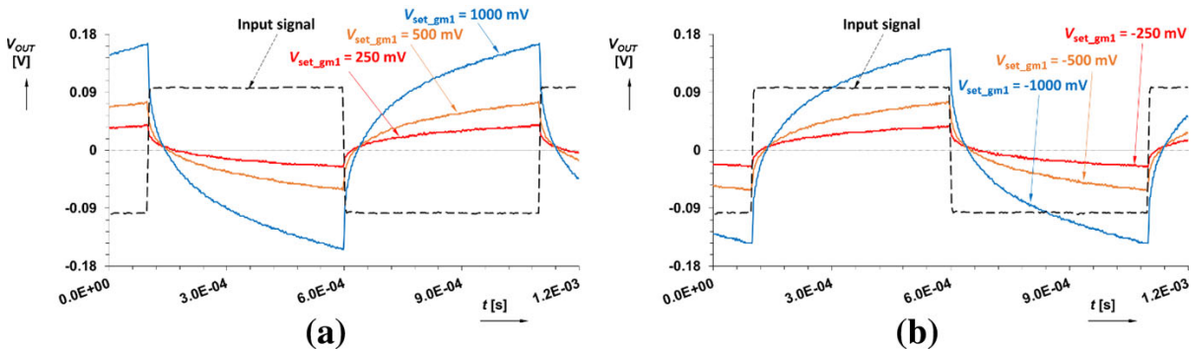

Fig. 18 Transient response of the integrational branch of the designed PID controller: **a** for positive polarity of V_{set_gm1}, **b** for negative polarity of V_{set_gm1}

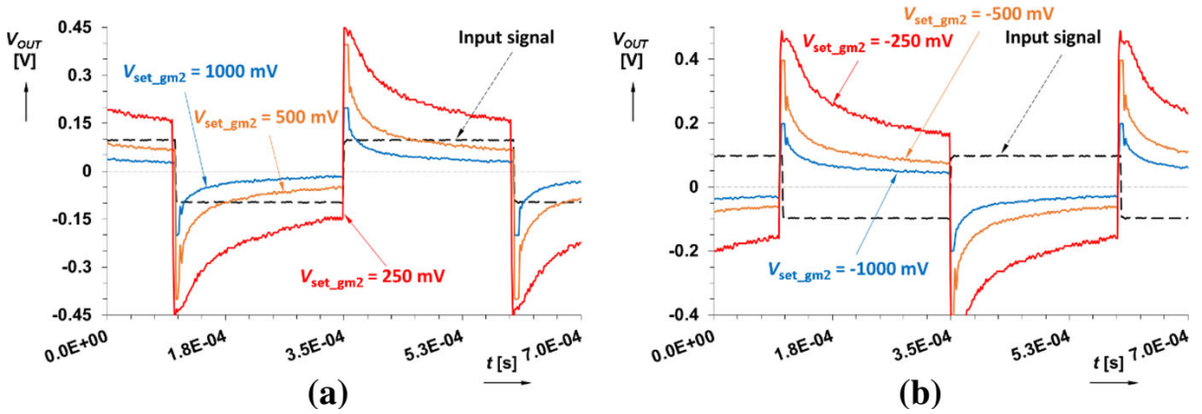

Fig. 19 Transient response of the differential branch of the designed PID controller: **a** for positive values of V_{set_gm2}, **b** for negative values of V_{set_gm2}

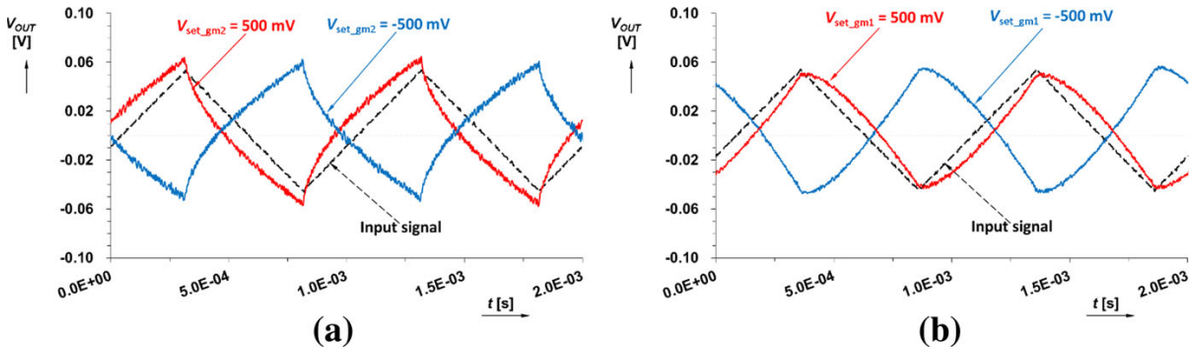

Fig. 20 Transient responses for triangular excitation of the PID controller (both polarities of $g_{m1,2}$) **a** integrational branch, **b** differential branch

The last measurement in time domain was made for a triangular input signal with two sets of control voltages ($V_{set\_gm1,2} = 500$ mV $\rightarrow g_{m1,2} \cong 1$ mS, $V_{set\_gm1,2} = -500$ mV $\rightarrow g_{m1,2} \cong -1$ mS). All of the following measurements are yielded for a frequency of 1 kHz and input voltage of 100 mV. Figure 20a shows results for testing the integrational branch, and Fig. 20b for measuring the differential branch (both with the same setting of V_{set} as in the measurements with rectangular input signal).

Features of the designed PID were also tested in AC domain. Magnitude and phase responses of particular blocks of the PID are shown in Figs. 21, 22, 23, 24 and 25 for several scenarios and both polarities. It can be seen, from the phase response, that particular settings of control voltage have no significant impact on the output phase,

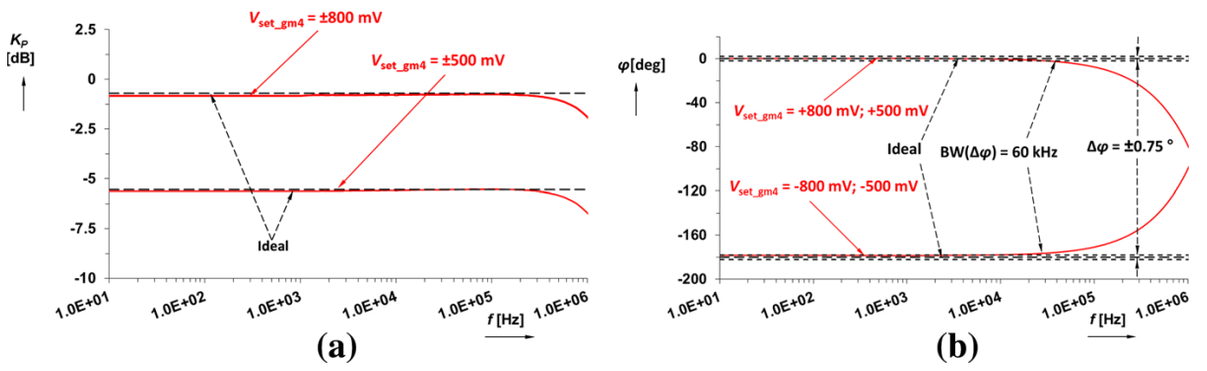

Fig. 21 Frequency responses of the proportional branch of the designed PID controller for both available polarities of V_{set_gm4}: **a** magnitude response, **b** phase response

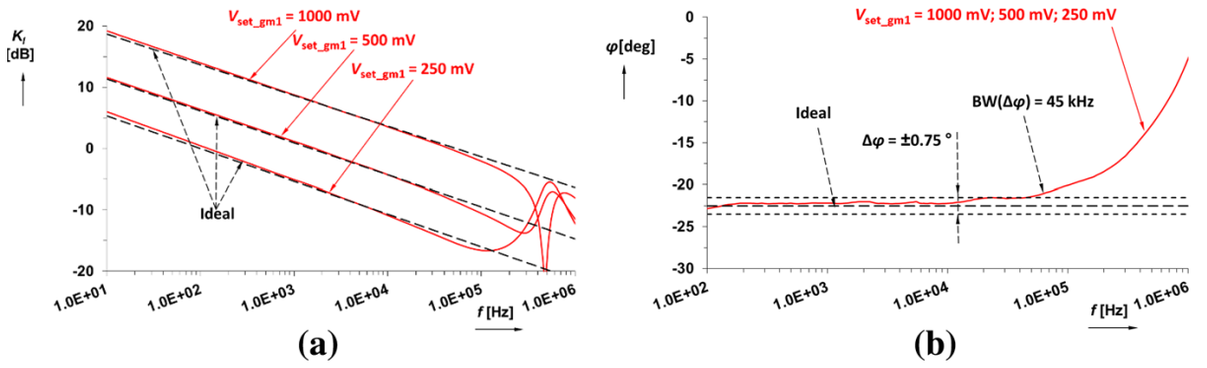

Fig. 22 Frequency responses of the integrational branch of the designed PID controller for positive polarity of V_{set_gm1}: **a** magnitude response, **b** phase response

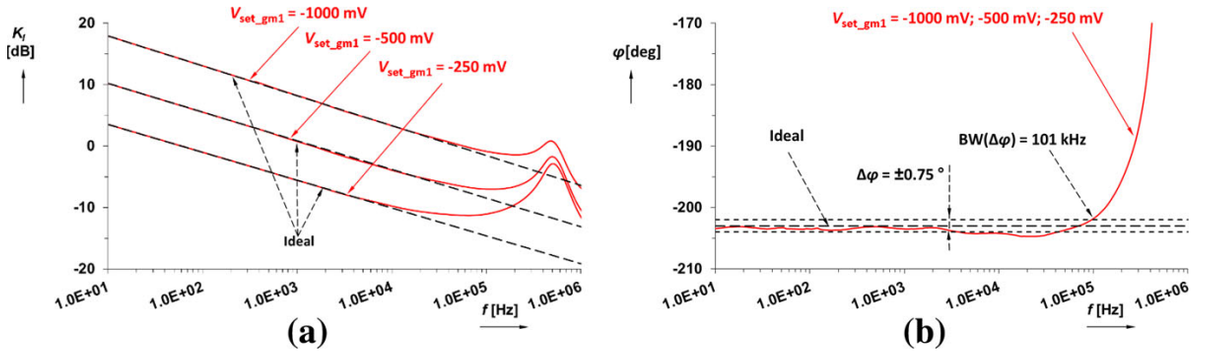

Fig. 23 Frequency responses of the integrational branch of the designed PID controller for negative polarity of V_{set_gm1}: **a** magnitude response, **b** phase response

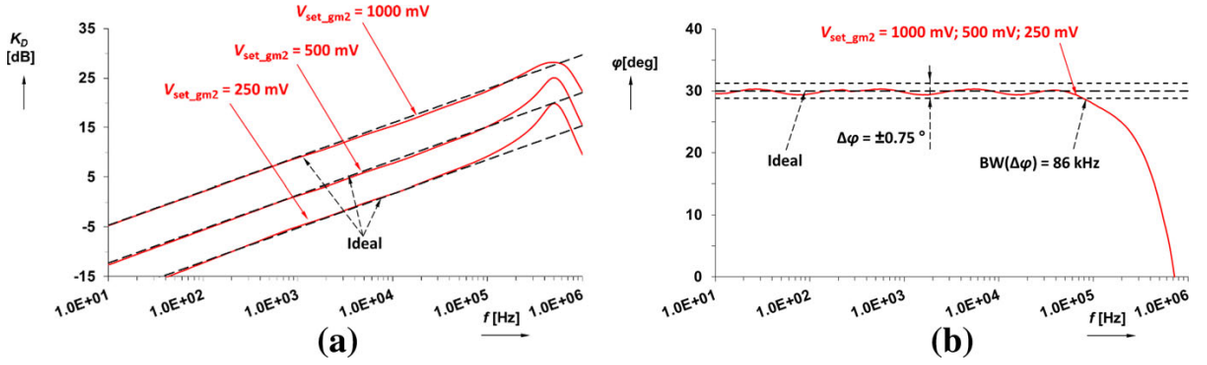

Fig. 24 Frequency responses of the differential branch of the designed PID controller for positive polarity of V_{set_gm2}: **a** magnitude response, **b** phase response

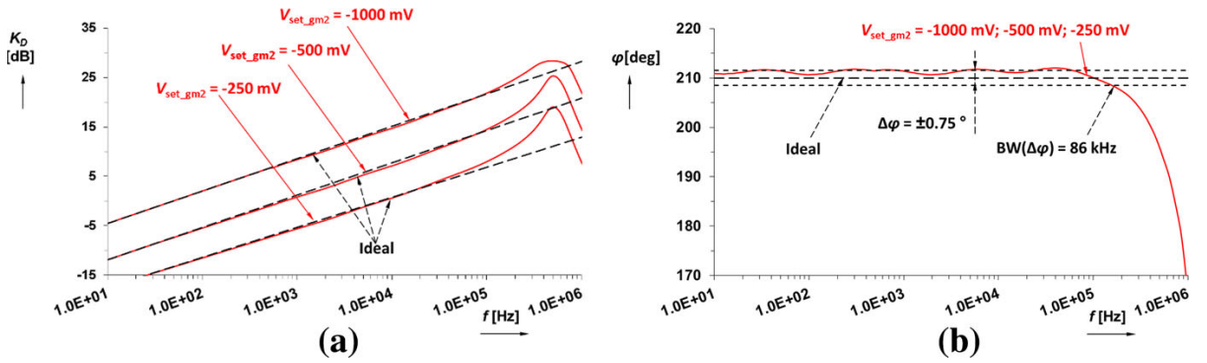

Fig. 25 Frequency responses of the differential branch of the designed PID controller for negative polarity of V_{set_gm2}: **a** magnitude response, **b** phase response

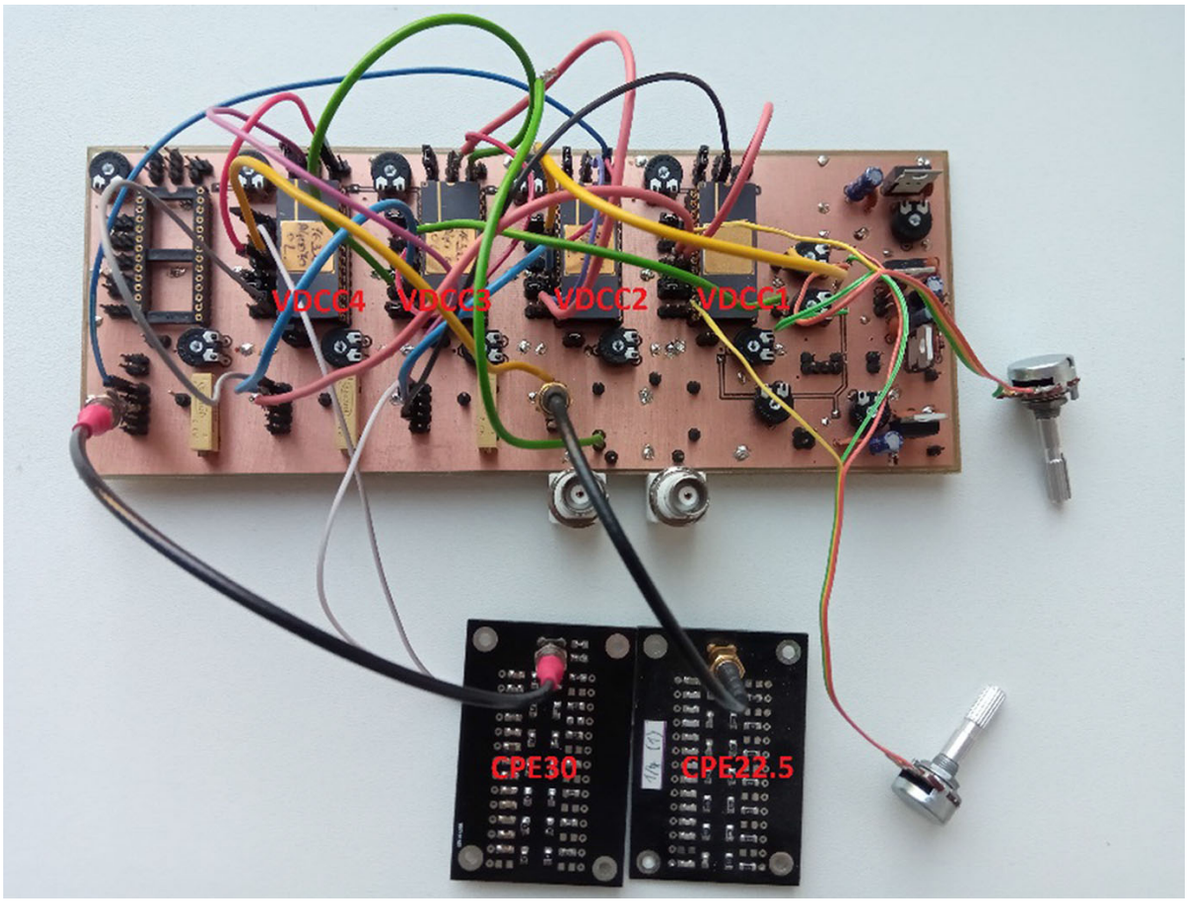

Fig. 26 The development board for five fabricated VDCC devices and tests of their applications

and therefore, curves are merged into one. The application of the CPEs and its impact on behavior of the final structure can be seen when the phase response fluctuates around a mean value with a certain phase ripple $\triangle\ \varphi$. BW($\triangle\ \varphi$) indicates the highest frequency band where phase ripple is $\triangle\ \varphi > 0.75°$.

4 Conclusion

The proposed structure of the constant phase element (CPE) was designed in the form of a ladder structure (Fig. 8) providing phase change of $\varphi = 30°$ and $\varphi = 22.5°$

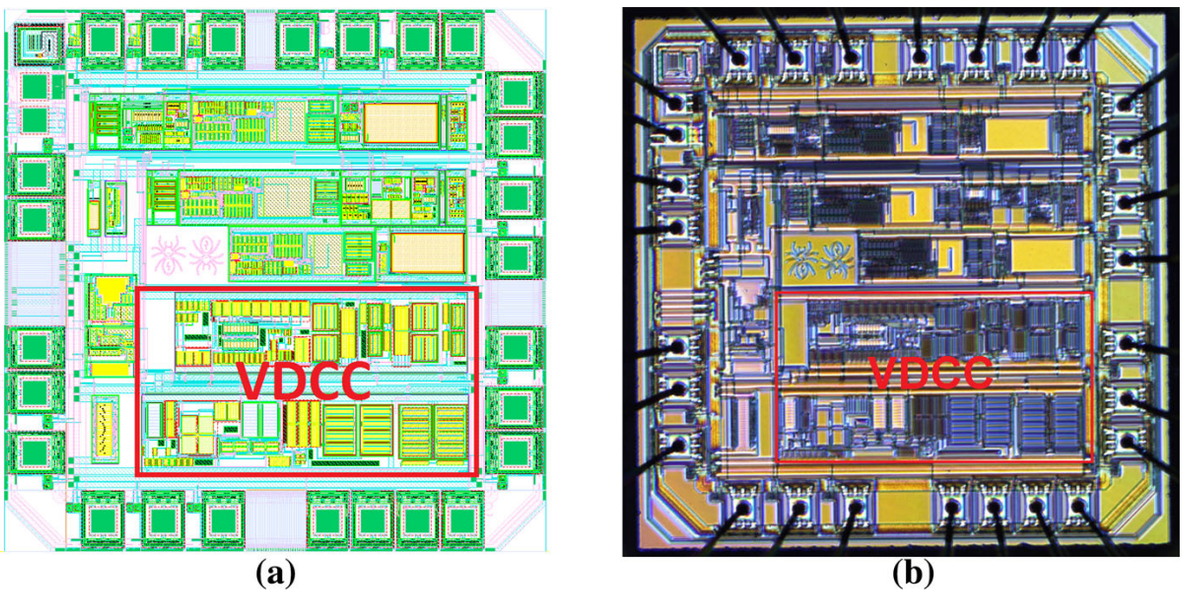

Fig. 27 The layout of the fabricated VDCC IC prototype (top layout frame 2×2 mm; cell area 0.79 mm^2): **a** Cadence IC5 software, **b** microphotograph

with very low phase ripple (about $\triangle\ \varphi = 0.75°$ in 4 decades) and it is described in Sect. 2. In particular, practical point of view of this design is discussed and the design guideline is given. Both designed CPEs were used in novel topology of the PI$^{\alpha}$D$^{\beta}$ regulator and can be seen in Fig. 26. This topology utilizes fabricated CMOS voltage differencing current conveyors (VDCC) as active elements (Fig. 27). The main benefits of VDCC consist in the independent electronic controllable transconductance $g_m(V_{set\_gm})$ and the resistance value $R_x(I_{set\_Rx})$ of the current input terminal X. Several of these parameters serve mainly for electronic control of the time constants and also polarities of transfers of the PID controller as well as the gain of the proportional branch. These interesting features of the newly proposed PID topology result from the special character of the developed VDCC device and its transconductance subpart (OTA) based on a voltage multiplier with a current output terminal [17, 38, 39]. No exception is that all passive elements are grounded. Regarding the designed PID topology, the improvement in the proposed structure is its low number of passive and active elements (only 4 passive elements and 4 active elements) in comparison with the already published solutions summarized in Table 1. The proposed PID operates up to several hundreds of kHz (with dc power consumption of 120 mW for $4 \times$ VDCC) that is given by technological bandwidth limitations of the fabricated VDCC. All results confirmed theoretical expectations of our design.

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B Integer-and Fractional-Order Integral and Derivative Two-Port Summations: Practical Design Considerations

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Author’s Contribution

Co-author of the conceptualization, methodology and development of the active realization of an analog board for interconnection of packages of modular cells. Formal analysis, research and data validation as well as taking part in a review and the editing process. Beyond fractional order elements, the reader can learn about practical solutions for the summing response of fractional and integer order differentiators, as well as a detailed Mathcad analysis of various functions Objective 1. Presented results in 3D plots indicate very interesting and useful responses (especially for filtering applications**,** so-called inverse response filters).

Author's contribution: 20 % (the second author).

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Integer-and Fractional-Order Integral and Derivative Two-Port Summations: Practical Design Considerations

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Abstract: This paper targets on the design and analysis of specific types of transfer functions obtained by the summing operation of integer-order and fractional-order two-port responses. Various operations provided by fractional-order, two-terminal devices have been studied recently. However, this topic needs to be further studied, and the topologies need to be analyzed in order to extend the state of the art. The studied topology utilizes the passive solution of a constant-phase element (with order equal to 0.5) implemented by parallel resistor–capacitor circuit (RC) sections operating as a fractional-order two-port. The integer-order part is implemented by operational amplifier-based lossless integrators and differentiators in branches with electronically adjustable gain, useful for time constant tuning. Four possible cases of the fractional-order and integer-order two-port interconnections are analyzed analytically, by PSpice simulations and also experimentally in the frequency range between 10 Hz and 1 MHz. Standard discrete active components are used in this design for laboratory verification. Practical recommendations for construction and also particular solutions overcoming possible issues with instability and DC offsets are also given. Experimental and simulated results are in good agreement with theory.

Keywords: constant phase element; differentiator; electronic adjusting; fractional-order element; integrator; summing of responses; two-port transfer; variable gain amplifier

1. Introduction

Circuit designs using fractional-order devices require a special type of analysis and evaluation because the resulting behavior of these systems is quite different and more complex than in cases of standard integer-order designs. Frequency responses influenced by the fractional-order behavior of used components are studied more frequently in recent years [1]. Many works in this field focus on novel solutions of integral and derivative two-ports (for example [2–9]), proportional integral and derivative controllers (for example [10–18] and so-called bilinear two ports [8,9,19–21] serving for various purposes. Two ports, known as integrators and differentiators, have started to be interesting for designers of fractional-order systems, and especially for proportional, integral and derivative controllers (PIDs). However, these systems are analyzed as complete solutions, and their transfer functions are considered in overall form (sum of all three responses).

The overview of typical examples dealing with the design of fractional-order integrators and differentiators (from the above discussed groups) is given in Table 1.

Table 1. Comparison of standalone fractional-order integrator/differentiator solutions and solutions included in designs of controllers and other relevant design approaches.

Reference	Design Target (Both = Integrator and Differentiator)	Simple Single Parameter Electronic Time Constant Tuning	Active Devices	Solution of Fractional-Order Part	Topological Circuit Complexity	SW Support not Required	Tested Operational Bandwidth	Application, if Any	Response Based on Combination of Integer and Fractional-Order
Integrators/Differentiators Only									
[2]	integrator	No	OAs	passive	Low	Yes	<1 MHz	N/A	-
[3]	both	Yes	DVCCTA	passive	Low	Yes	<100 kHz	N/A	-
[4]	both	No	CMOS current mirrors	active	Low	Yes	<100 Hz	Sum of reconfigurable filtering responses	No
[5]	integrator	No	CMOS OTAs	active	Medium	Yes	<1 kHz	N/A	-
[6]	both	No	CFOAs	active	Medium	Yes	<100 kHz	N/A	-
[7]	both	No	Single EX-CCII	passive	Low	Yes	<1 kHz	PID	No
[8]	both	No	CMOS block	active	Low	Yes	<100 Hz	high-pass/low-pass filter	No
[9]	integrator	Yes	CCII+, VGA	active	High	Yes	<10 MHz	N/A	-
Integrators/Differentiators in Controllers									
[10]	integrator	No	OAs	passive	Low	Yes	<10 kHz	I controller	-
[11]	both	No	OAs	passive	Low	Yes	<100 Hz	PID	No
[12]	both	N/A	FPAA (OAs)	active	High	No	<100 Hz	PID	No
[13]	both	No	CMOS OTAs	active	Medium	Yes	<1 kHz	PID	No
[14]	both	No	CMOS VDCCs	passive	Low	Yes	<1 MHz	PID	No
[15]	both	No	MCDUs	active	Medium	Yes	<10 MHz	PI/D	No
[16]	both	N/A	FPGA/DSP *	active	High	No	<tens of MHz	PID	No
[17]	both	N/A	FPGA/DSP *	active	High	No	<tens of MHz	N/A	-
Bilinear Synthesis of Integrators/Differentiators									
[8]	both	No	CMOS block	active	Low	Yes	<1 MHz	Active CPE	-
[18]	both	No	CMOS OAs	active	High	Yes	<1 kHz	PI controller	No
[19]	integrator	No	CMOS OTAs	active	High	Yes	<10 MHz	N/A	-
[20]	both	No	CFOAs	active	Medium	Yes	<100 kHz	N/A	-
[21]	integrator	No	OTAs	active	Medium	Yes	<100 kHz	N/A	-

Table 1. *Cont.*

Reference	Design Target (Both = Integrator and Differentiator)	Simple Single Parameter Electronic Time Constant Tuning	Active Devices	Solution of Fractional-Order Part	Topological Circuit Complexity	SW Support not Required	Tested Operational Bandwidth	Application, if Any	Response Based on Combination of Integer and Fractional-Order
Proposed									
[3,5,7,9]	both	Yes	OAs, VGAs	passive	Low	Yes	<1 MHz	Sum of integer- and fractional-order responses	Yes

* general functional blocks; N/A—information not shown, not available; CCII+—current conveyor of second generation; CFOA—current feedback operational amplifier; DVCCTA—differential voltage current controlled current conveyor transconductance amplifier; EX-CCII—extra inputs current conveyor of second generation; FPAA—field programmable analog array; FPGA/DSP—field programmable gate array/digital signal processing; MCDU—modified current differencing unit; OA—operational amplifier; OTA—operational transconductance amplifier; VDCC—voltage differencing current conveyor; VGA—variable gain amplifier; low—less than 6 active devices (less than 6 passive devices, solution of CPE excluded), medium—between 6 and 10 active devices, high—more than 10 active devices.

D. Mondal et al. [2] brought a solution of the lossless integrator using a fractional-order passive element (FOE), known also as constant phase element (CPE) as a part of feedback loop of operational amplifier (OA) followed by inverter. However, adjustability and other features (two different slopes in magnitude frequency responses, various starting and final phase shifts in observed bandwidth, etc.) are not studied. D. Goyal et al. [3] presents integrators/differentiators implemented by complex active CMOS circuitry with the benefit of simple electronic reconfiguration. A similar approach was used by G. Tsirimokou et al. [4] where resulting integrators/differentiators are used for the design of a special type of filter performing also the sum/subtraction of current outputs. The synthesis of an active emulator of FOE based on operational transconductance amplifiers and its implementation in an OA-based lossless integrator is shown by G. Tsirimokou et al. [5]. Special active building blocks used in works [3–5,8] utilize approximation of the fractional-order behavior by higher-integer-order filtering responses allowing the electronic configuration of transfer coefficients (numerator/denominator). Similarly, G. Tsirimokou et al. [6], there is a discrete solution of this topology using passive parameters for appropriate configuration of the transfer. Topology presented by S. Kapoulea [7] represents one from the simplest examples of device using passive form of FOE-based on serial/parallel interconnections of RC segments. R. Sotner et al. [9] introduces method for the electronic rescalability of the operational bandwidth of the fractional-order integrator, by single DC voltage controlling several capacitance multipliers. Similarly to G. Tsirimokou et al. [6], this topology uses passive parameters for the setting of the response approximating required fractional-order behavior. Note that except R. Sotner et al. [9], there was no attempt to obtain single a parameter electronic adjustability of time constant in the area of fractional-order two-ports (integrators/differentiators).

Many interesting solutions of two-port interconnections have been presented as parts of various fractional-order controllers [10–18]. Many of them are using standard topologies based on OA [10,11] because of their simplicity. Some approaches target on extensive and complex design, based on field programmable analog arrays (FPAAs) [12] and field programmable gate arrays (FPGAs) [16], [17] because of their programmability. Moreover, FPGA represents a digital-only solution of the design. It allows the integration of highly complex topologies [12,16,17], but certain latency and delay of processing may occur in some cases. However, a significant drawback of these concepts is the necessity of software development and also quite high costs in comparison to a simple analog solution. Special analog active devices (with controllable internal parameters) used in the synthesis of controllers bring certain advantages in the simplification of the design and possibility of electronic adjustability/reconfigurability at the same time [13–15].

So-called bilinear synthesis brought significant contributions to the adjustability of the features of fractional-order devices [8,18–21]. Electronic tuning of zero and pole frequencies allows one to form an almost arbitrary frequency response with very simple and immediate reconfiguration [8,19–21].

Analysis of known solutions leads to the following conclusions:

(a) Many proposed circuitries (except FPAA, FPGA-based) have quite complex topology, with many active and/or passive elements [9,12,16–19], especially circuits with fractional-order behavior and approximations by higher-order filters [3,5,6,13] or chain of bilinear segments [8,9,14,15,18–21],
(b) some concepts require software programming [12,16,17],
(c) tested operational bandwidth is quite narrow in many cases [3–5,7,8,11–13,18],
(d) summing of fractional-order as well as integer-order two ports was not analyzed deeply in the past,
(e) single-parameter electronic adjustment of the time constant of the resulting response of two-port summing was not studied in the past, except R. Sotner et al. [9], but the overall circuit topology is based upon a chain of bilinear sections, and therefore, it is not one of the simplest solutions

Despite the presence of various solutions of the above-mentioned two-ports, the effects of their mutual interconnections are studied rarely [4,8]. The most known cases of integral and derivative

responses used simultaneously can be found in the field of controllers [7,10–16,18]. However, a detailed study of resulting responses is often omitted.

The first work (Tsirimokou et al. [22]), where various simple interconnections of fractional-order devices has been studied, targets on combinations of two-ports. This work gives the evaluation of the resulting impedance functions of serial/parallel interconnections of fractional-order capacitors (RC approximants), where each two-terminal is actually represented by an active solution allowing simple electronic configurability and also floating implementation. Experimental tests were performed for very low frequencies (<1 kHz). Kartci et al. [23] introduced work dealing with more complex interconnections of real solid-state, fractional-order two-terminals. However, despite further attempts in the synthesis of passive [24,25] or active [26] two-terminals, there are no attempts studying both simple and complex interconnections of fractional-order and integer-order two-ports. Moreover, the area of theoretical knowledge of fractional-order systems significantly extends into practical industrial applications [27].

To the best of the authors' knowledge, a similar study targeting on interconnections of fractional and integer order two-ports has not been presented in literature. However, there are many particular cases that should be studied. This work focuses deeply on the behavior of the sum of two branches, including fractional-order, two-port (differentiator or integrator) and integer-order two port (differentiator or integrator). Features of resulting responses are studied theoretically, by PSpice simulation, and also experimentally. The practical notes for the construction of these interconnections of two-ports are also given. The initial work in this field was presented as conference paper [28]. However, very limited example of test cases was presented. In the case of this paper, the setting is totally different and also the types of active devices are not the same.

This work targets on:

(a) the derivation of analytical expressions for mixed transfers, including sum of integer and fractional-order two-ports,
(b) a single parameter electronic adjustment of the respective time constants,
(c) the practical verification and also precautions of real implementation,
(d) an extension of the state of the art in the field of serial/parallel interconnections of fractional-order two-terminal passive elements [22,23] to the two-port area.

The rest of this paper has the following organization: Section 2 describes the general block concept of the tested two-port interconnections. Section 3 shows features of the CPE element (RC approximant) used in analyzed cases. Section 4 presents four possible combinations of integrator and differentiator (fractional- and integer-order transfer branch) when summing their output responses, and it shows their analytical analysis. Practical issues in tested topologies, as well as possible solutions/compensations of these effects are discussed in Section 5. Section 6 introduces experimental results, and Section 7 concludes this work.

2. General Concept of Two-Port Interconnection

This work introduces the way of analyzing behavior of the resulting response of a sum of lossless integrator and differentiator where each of them has integer as well as fractional-order character (Figure 1). We will also observe the impact of the gain variation (designated as A_1 and A_2 in Figure 1) on the features of each path. We decided to study four particular cases: (a) integer-order integrator + fractional-order integrator, (b) integer-order differentiator + fractional-order differentiator, (c) integer-order integrator + fractional-order differentiator, (d) integer-order differentiator + fractional-order integrator.

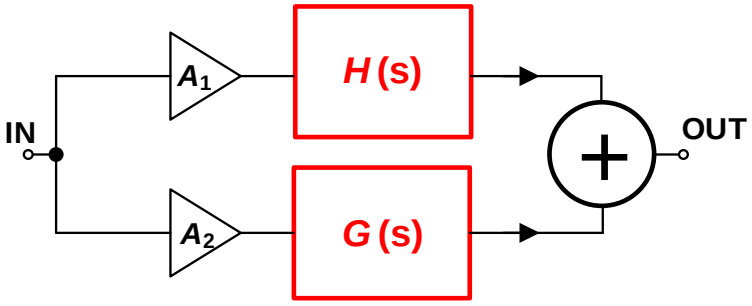


Figure 1. General concept of all four analyzed systems (responses).

The transfer of the generalized system has form:

$$K_C(s) = A_1 \cdot H(s) + A_2 \cdot G(s) \tag{1}$$

where partial transfers $H(s)$ and $G(s)$ are as follows:

$$H_{\text{int\_C}}(s) = \frac{1}{\tau_1 s} \tag{2}$$

$$G_{\text{int\_CPE}}(s) = \frac{1}{\tau_2 s^{\alpha}} \tag{3}$$

$$H_{diff\_C}(s) = \tau_1 s \tag{4}$$

$$G_{diff\_CPE}(s) = \tau_2 s^{\alpha} \tag{5}$$

$$H_{diff\_C}(s) = \tau_1 s \tag{6}$$

$$G_{\text{int\_CPE}}(s) = \frac{1}{\tau_2 s^{\alpha}} \tag{7}$$

$$H_{\text{int\_C}}(s) = \frac{1}{\tau_1 s} \tag{8}$$

$$G_{diff\_CPE}(s) = \tau_2 s^{\alpha} \tag{9}$$

where the particular index of $H(s)$ and $G(s)$ indicates the character of the accumulating device used in a particular two-port, and $\tau_{1,2}$ are initial values of the time constants.

Commercially-available, active devices can be used for purposes of practical verification of the concept from Figure 1 [29]. Variable gain amplifiers (VGAs) providing control of A_1 and A_2 gains will be based on VCA810 devices [30], the standard concept of the integrator and differentiator topology will utilize the LT1364 operational amplifier [31], and the sum operation is easily achievable by an AD8130 element [32]. In order to obtain fractional-order integrator or differentiator topology, a fractional-order element is required. The Constant Phase Element (CPE) is one of the possibilities described in the next section. The following subsections describe each of the four considered topologies, together with the most significant simulation and experimental results.

3. Passive Solution of Constant Phase Element

We selected CPE having order $\alpha = 0.5$ with $C_\alpha = 56$ μF/s$^{1/2}$ for all experimentally studied cases (presented in Section 6). Its practical implementation by RC passive topology is shown in Figure 2, as well as its ideal and simulated magnitude and phase impedance characteristics. The phase accuracy of this CPE reaches $\Delta\varphi_\alpha = \pm 2°$ in the theoretical operational bandwidth between 1 Hz and 3 MHz. The design was performed by the algorithm explained in several works in detail [14,33,34].

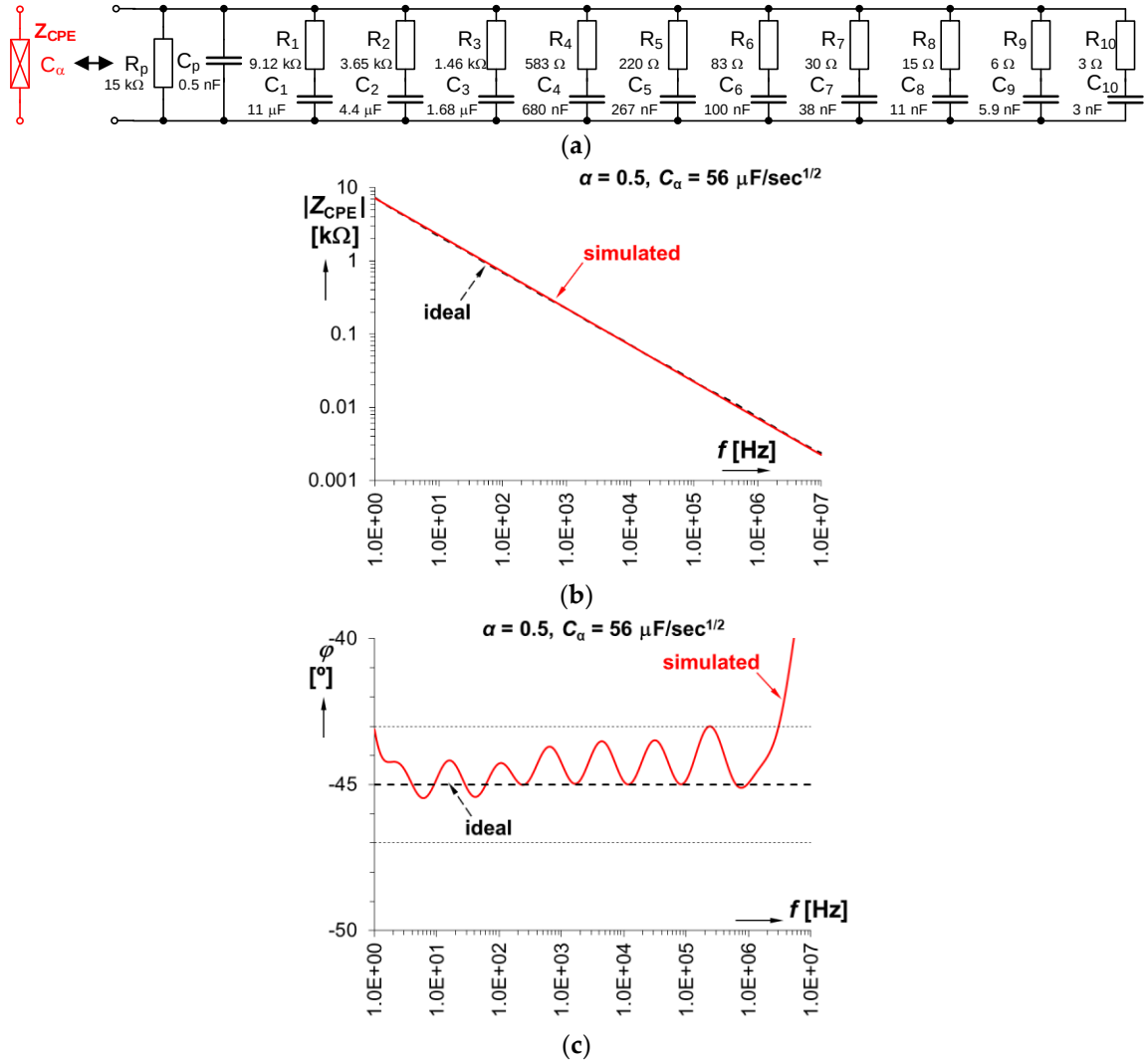


Figure 2. Practical implementation of the Constant Phase Element (CPE) solution from resistor–capacitor circuit (RC) segments: (**a**) circuit topology; (**b**) magnitude of impedance; (**c**) phase of impedance.

4. Analytical Analysis of Two-Port Interconnections

We divided ideal analysis to four sections in accordance to discussion in Section 2. Each interconnection is represented by real circuit topology, including all used active devices and values of used passive elements, as well as compensating elements improving stability as will be explained later. Note that compensating passive elements, drawn in the figures by dashed lines, are excluded from analytical analysis because of simplicity. The following ideal analyses use $\tau_{1(\text{integer})} = 100$ µs, $\tau_{2(\text{fractional/CPE})} = 5.6$ ms and fixed $A_1 = A_2 = 1$.

4.1. Sum of Integer and Fractional-Order Integrator Responses

Practical circuitry implementing the fractional-order integrator and integer-order integrator derived from the general concept in Figure 1 is shown in Figure 3. Its transfer function is given by:

$$K_{I\_I}(s) = \frac{A_1}{\tau_1 s} + \frac{A_2}{\tau_2 s^{\alpha}} \tag{10}$$

Its representation in complex form is quite extensive:

$$K_{I\_I}(\omega) = \frac{1}{\tau_1\tau_2\omega^{1+\alpha}}\left\{A_2\tau_1\omega\sin\left((1+\alpha)\frac{\pi}{2}\right) + j\left[A_2\tau_1\omega\cos\left((1+\alpha)\frac{\pi}{2}\right) - A_1\tau_2\omega^{\alpha}\right]\right\} \quad (11)$$

Magnitude and phase part can be expressed as, respectively:

$$\left|K_{I\_I}(\omega)\right| = \frac{1}{\tau_1\tau_2\omega^{1+\alpha}}\sqrt{\left[A_2\tau_1\omega\sin\left((1+\alpha)\frac{\pi}{2}\right)\right]^2 + \left[A_2\tau_1\omega\cos\left((1+\alpha)\frac{\pi}{2}\right) - A_1\tau_2\omega^{\alpha}\right]^2} \quad (12)$$

$$\varphi_{I\_I}(\omega) = \tan^{-1}\left[\frac{A_2\tau_1\omega\cos\left((1+\alpha)\frac{\pi}{2}\right) - A_1\tau_2\omega^{\alpha}}{A_2\tau_1\omega\sin\left((1+\alpha)\frac{\pi}{2}\right)}\right] \quad (13)$$

The Mathcad analysis of ideal transfer function (10) is shown in Figure 4 as three dimensional (3D) plots. Variation of order α between 0 and 1 indicates a clear point of break where the slope divides into two parts (integer-order low-frequency zone and fractional-order high-frequency zone), and the movement of position of this intentional zero from high frequencies to low frequencies, as well as increasing the character of the corner phase shift at the end of the operational band (from −90° up to 0°).

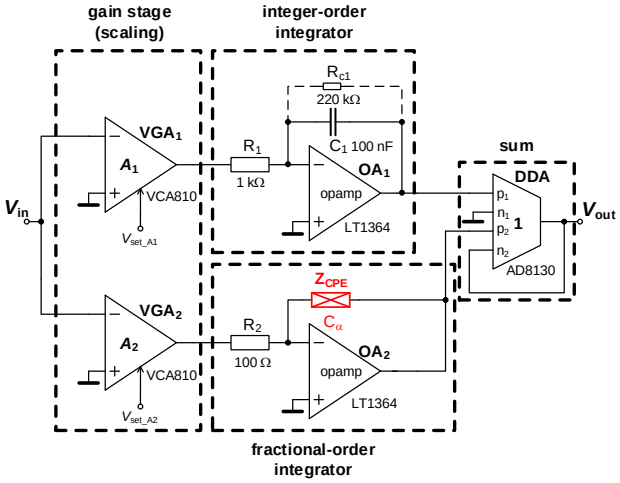
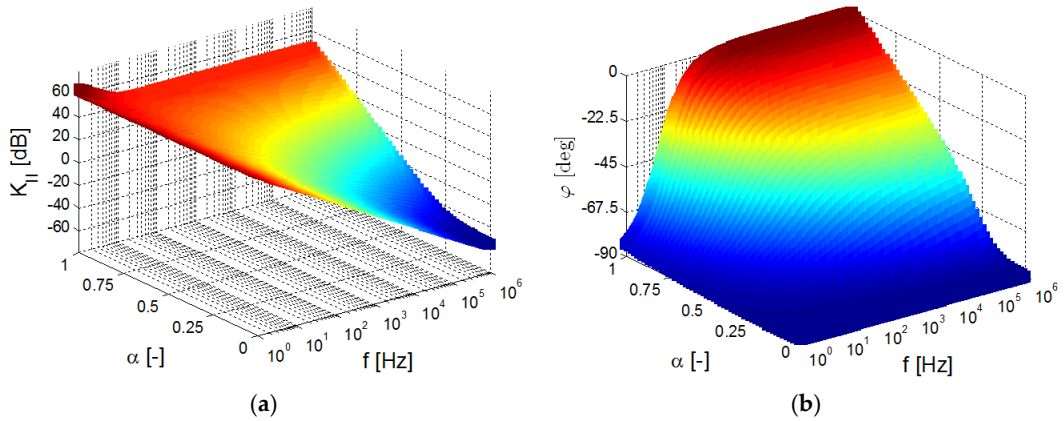


Figure 3. Practical solution of circuitry providing summing responses of the fractional- and integer-order integrators.



(**a**) (**b**)

Figure 4. The three dimensional (3D) plot of studied ideal transfer response (10) in dependence on the value of the α variable: (**a**) magnitude vs. order vs. frequency dependence, (**b**) phase vs. order vs. frequency dependence.

4.2. Sum of Integer and Fractional-Order Differentiator Responses

Figure 5 shows interconnection resulting from the summing operation of integer and fractional-order differentiator responses. The transfer function can be expressed as:

$$K_{D\_D}(s) = A_1\tau_1 s + A_2\tau_2 s^{\alpha} \tag{14}$$

The rearrangement into complex form leads to:

$$K_{D\_D}(\omega) = A_2\tau_2\omega^{\alpha}\cos\left(\frac{\alpha\pi}{2}\right) + j\left[A_1\tau_1\omega + A_2\tau_2\omega^{\alpha}\sin\left(\frac{\alpha\pi}{2}\right)\right] \tag{15}$$

and after separation to magnitude and phase response we obtain:

$$\left|K_{D\_D}(\omega)\right| = \sqrt{\left[A_2\tau_2\omega^{\alpha}\cos\left(\frac{\alpha\pi}{2}\right)\right]^2 + \left[A_1\tau_1\omega + A_2\tau_2\omega^{\alpha}\sin\left(\frac{\alpha\pi}{2}\right)\right]^2} \tag{16}$$

$$\varphi_{D\_D}(\omega) = \tan^{-1}\left[\frac{A_1\tau_1\omega + A_2\tau_2\omega^{\alpha}\sin\left(\frac{\alpha\pi}{2}\right)}{A_2\tau_2\omega^{\alpha}\cos\left(\frac{\alpha\pi}{2}\right)}\right] \tag{17}$$

The Mathcad analysis of the transfer function (14) is shown in Figure 6. It shows that order variation (the same as in the previous case) causes a very similar point of break on the magnitude slope and occurrence of zero at low frequencies (especially for orders near to 1), and the cut of the plane projection of the phase response confirms that this starting phase value (low frequencies) clearly depends upon the value of the α order.

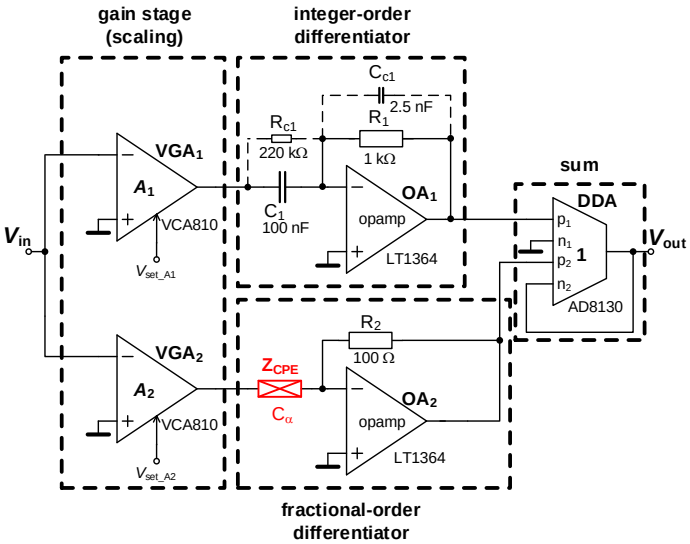


Figure 5. Practical solution of the summing response of fractional- and integer order differentiator.

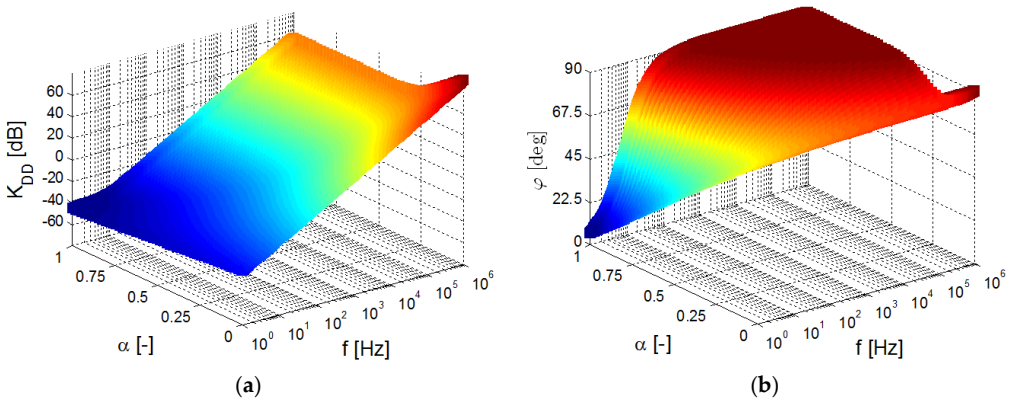


Figure 6. 3D plot of the studied ideal transfer response (14) in dependence on the value of the α variable: (**a**) magnitude vs order vs frequency dependence, (**b**) phase vs order vs frequency dependence.

4.3. Sum of Integer-Order Integrator and Fractional-Order Differentiator Responses

This topology has behavior indicating a significant global minimum of the ideal transfer magnitude because the decreasing and increasing magnitude in frequency response is given by the interconnection of the integrator and differentiator (Figure 7). The response has this form:

$$K_{I\_D1}(s) = \frac{A_1}{\tau_1 s} + A_2 \tau_2 s^{\alpha} \tag{18}$$

that can be easily modified to the complex expression:

$$K_{I\_D1}(\omega) = \frac{1}{\omega\tau_1}\left\{\omega^{1+\alpha}\tau_1\tau_2 A_2 \sin\left((1+\alpha)\frac{\pi}{2}\right) - j\left[\omega^{1+\alpha}\tau_1\tau_2 A_2 \cos\left((1+\alpha)\frac{\pi}{2}\right) + A_1\right]\right\} \tag{19}$$

and the resulting magnitude and phase responses of the two-port are:

$$\left|K_{I\_D1}(\omega)\right| = \frac{1}{\omega\tau_1}\sqrt{\left[\omega^{1+\alpha}\tau_1\tau_2 A_2 \sin\left((1+\alpha)\frac{\pi}{2}\right)\right]^2 + \left[\omega^{1+\alpha}\tau_1\tau_2 A_2 \cos\left((1+\alpha)\frac{\pi}{2}\right) + A_1\right]^2} \tag{20}$$

$$\varphi_{I\_D1}(\omega) = \tan^{-1}\left[\frac{\omega^{1+\alpha}\tau_1\tau_2 A_2 \cos\left((1+\alpha)\frac{\pi}{2}\right) + A_1}{\omega^{1+\alpha}\tau_1\tau_2 A_2 \sin\left((1+\alpha)\frac{\pi}{2}\right)}\right] \tag{21}$$

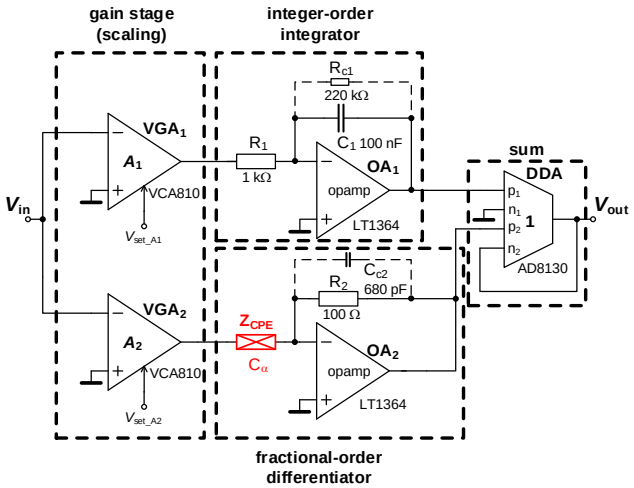


Figure 7. Practical solution of the summing response of fractional-order differentiator and integer order integrator.

The ideal analysis of (18) shown in Figure 8 indicates two-sides of the magnitude response with different slopes and significant local minimum. The phase plot confirms the impact of the order on the phase value in high-frequency corner (between 0° and 90°).

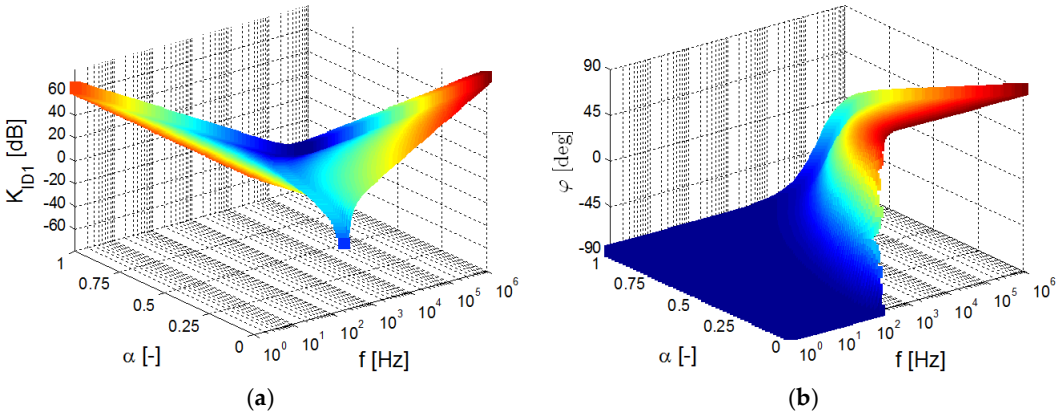


Figure 8. The 3D plot of studied ideal transfer response (18) in dependence on value of the α variable: (**a**) magnitude vs order vs frequency dependence, (**b**) phase vs order vs frequency dependence.

4.4. Sum of Fractional-Order Integrator and Integer-Order Differentiator Responses

The last considered combination of integer-order and fractional-order response is shown in Figure 9. The resulting frequency response is quite similar to the previous case:

$$K_{I\_D2}(s) = A_1\tau_1 s + \frac{A_2}{\tau_2 s^{\alpha}} \tag{22}$$

again, we can modify it to the complex form:

$$K_{I\_D2}(\omega) = \frac{1}{\omega^{\alpha}\tau_2}\left\{A_2\cos\left(\frac{\alpha\pi}{2}\right) + j\left[\omega^{1+\alpha}\tau_1\tau_2 A_1 - A_2\cos\left(\frac{\alpha\pi}{2}\right)\right]\right\} \tag{23}$$

and we can express the corresponding magnitude and phase responses:

$$\left|K_{I\_D2}(\omega)\right| = \frac{1}{\omega^{\alpha}\tau_2}\sqrt{\left[A_2\cos\left(\frac{\alpha\pi}{2}\right)\right]^2 + \left[\omega^{1+\alpha}\tau_1\tau_2 A_1 - A_2\cos\left(\frac{\alpha\pi}{2}\right)\right]^2} \tag{24}$$

$$\varphi_{I\_D2}(\omega) = \tan^{-1}\left[\frac{\omega^{1+\alpha}\tau_1\tau_2 A_1 - A_2\cos\left(\frac{\alpha\pi}{2}\right)}{A_2\cos\left(\frac{\alpha\pi}{2}\right)}\right] \tag{25}$$

The 3D plot in Figure 10 also reports the significant global minimum of transfer (as expected). However, the sides of both slopes are opposite with respect to the previous case. The cut in phase projection shows the initial phase value (low-frequency corner) dependence on the order (start between −90° and 0°).

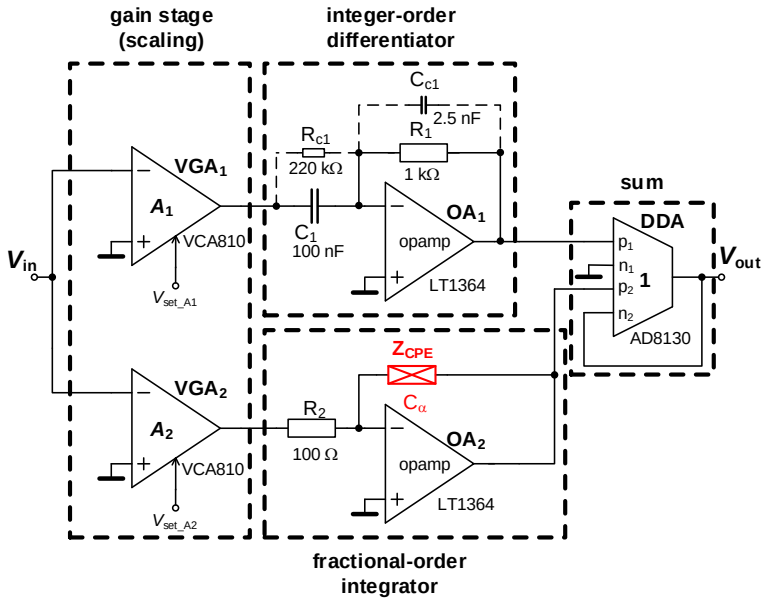


Figure 9. Practical solution of the summing response of fractional-order integrator and integer-order differentiator.

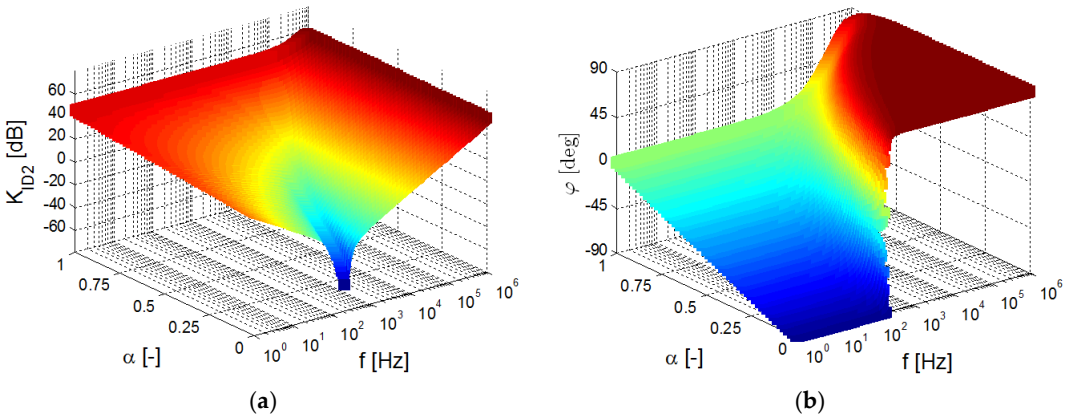


Figure 10. The 3D plot of the studied ideal transfer response (22) in dependence on the value of α variable: (**a**) magnitude vs order vs frequency dependence, (**b**) phase vs order vs frequency dependence.

5. Solving Non-Ideal Issues during the Tests

Note that the bridging resistor R_{c1}, being part of each of the presented summing solutions, intentionally limits the direct current (DC) gain of OA$_1$ to a finite value (≅200) in order to minimize the impacts of the saturation of the output because of nonzero DC offset caused by real asymmetry of the active elements. Moreover, effects of high-gain blocks, as well as remaining DC offsets, require manual compensations by DC voltage applied against real DC offset, as shown in Figure 11. These compensations are required in both paths of the studied topology. In our case, the input DC offsets reach values of tens of mV, approximately. However, it was sufficiently high to cause saturation ($V_{out} = V_{DD}$ or V_{SS}) of the OA output. Therefore, the compensation was provided really carefully. Note that the output DC shift above ±50 mV causes a significant effect on the frequency response accuracy.

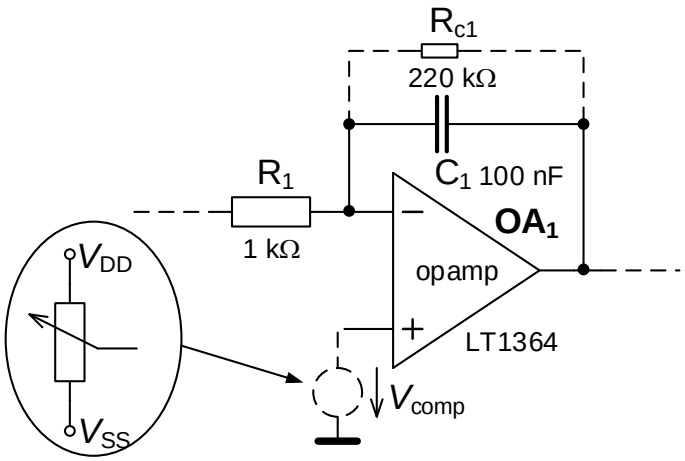


Figure 11. Principle of intentional DC gain limitation and compensation of DC offset and asymmetry of inputs in the case of integer-order branch given as an example.

Moreover, also damping of unintentional oscillations should be done by a parallel connection of the capacitor to the feedback resistor in the OA network, as shown in Figure 12. Note that gain caused by the derivative character of the branch increases with frequency (more than 40 dB above 100 kHz). The compensation of instability by additional C_{C1} and C_{C2} elements was prepared to suppress the resonant peak approximately between 200 and 300 kHz, as shown in Figures 5, 7 and 9. Despite quite high values of C_C-s, the value of this intentional frequency zero is quite high because of parallel resistors having low value (100 Ω and 1 kΩ). The approximate value of compensating zero frequency can be calculated as $f_{zC} = 1/(2{\cdot}\pi{\cdot}R_1C_{C1})$. For values included in Figure 12 it is 63 kHz. It indicates that influences causing possible instability and oscillations above 100 kHz are sufficiently suppressed.

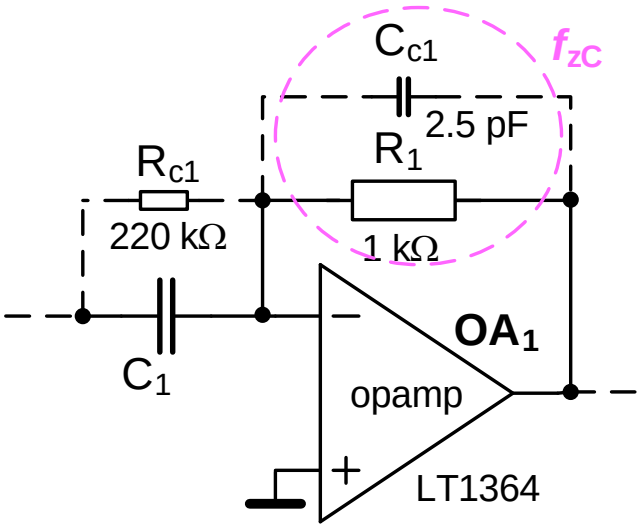


Figure 12. An example of frequency compensation of instability in integer-order branch given as an example.

6. Experimental Analysis

Two-ports discussed above were analyzed in PSpice software and also experimentally with real devices. We used oscilloscope Keysight DSOX3022T with the Frequency Response Analysis (FRA) option [35] for time domain as well the as frequency domain testing. The input signal level used in tests was approximately 30 $mV_{P\text{-}P}$ because of the significant change of gain, and it was constant in the whole observed band (20 Hz–1 MHz). The simultaneous time-domain and frequency-domain

measurements, enabled by this oscilloscope during the point-to-point FRA analysis, were necessary due to clear visibility of the correct setting of DC offset error compensation.

We can calculate initial time constants of the OA-based integrator/differentiator directly from values shown in Figures 3, 5, 7 and 9: $\tau_{1(\text{integer})} = 100$ s ($R_1 \times C_1 = 1$ kΩ × 100 nF), $\tau_{2(\text{fractional/CPE})} = 5.6$ ms ($R_2 \times C_\alpha = 100\ \Omega \times 56\ \mu\text{F/s}^{1/2}$). The driving voltages $V_{\text{set\_A1}}$ and $V_{\text{set\_A2}}$ for the time constant adjustment by gains A_1 and A_2 are considered between 0.85 and 1.35 V ($A_{1,2}$ between 0.5 and 5 because $A_{1,2} = 10^{(2\cdot(\text{Vset\_A1,2} - 1))}$ [30]) in order to observe a one-decade change of gain. However, increased gain requires compensation of instability as well as DC offset (VGA output offset depends on actual gain), as discussed above. Particular values of gains $A_{1,2}$ are noted directly in presented graphs. Note that our design targets are on the low-frequency band of operation (application field between 100 Hz and 100 kHz) because of expected limits (DC offset impacts for high gain scale, instability) of active devices as well as simpler design for our exemplary purposes.

6.1. Analysis of Integer-and Fractional-Order Integrators and Differentiators

The frequency responses of key parts of the system (integrators/differentiators using integer- or fractional-order capacitor) are studied before analysis of the response of the whole system (Figure 1). Results are shown in Figure 13 for the integral branch and in Figure 14 for the derivative branch. Above discussed parameters of time constants are valid also for this case. The operational bandwidth of the integrators (considering phase changes) is limited into the range approximately between 50 Hz and 200 kHz. The operational band of differentiators is significantly lower (only 50 Hz–10 kHz) due to high-frequency limitations and parasitic poles (and their intentional compensation) in case of a real transfer function.

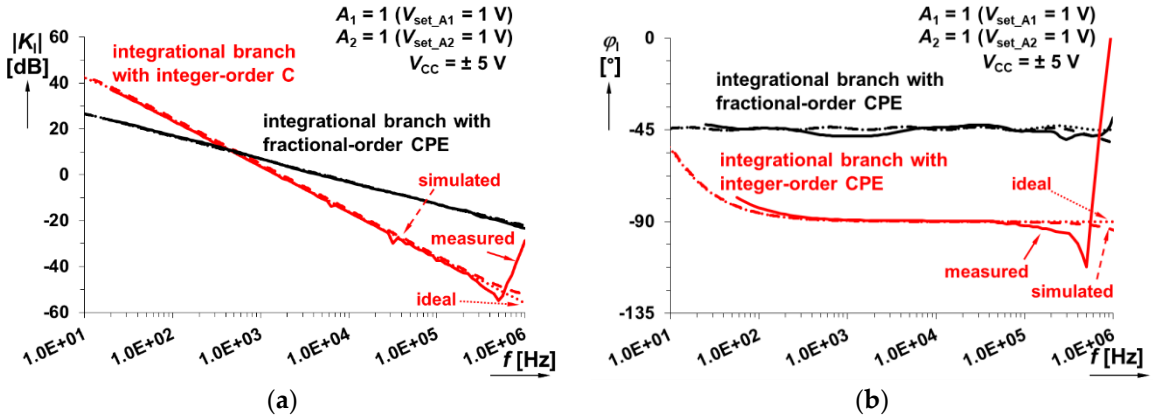


Figure 13. Frequency response of integer-order and fractional-order integrator: (**a**) magnitude responses; (**b**) phase responses.

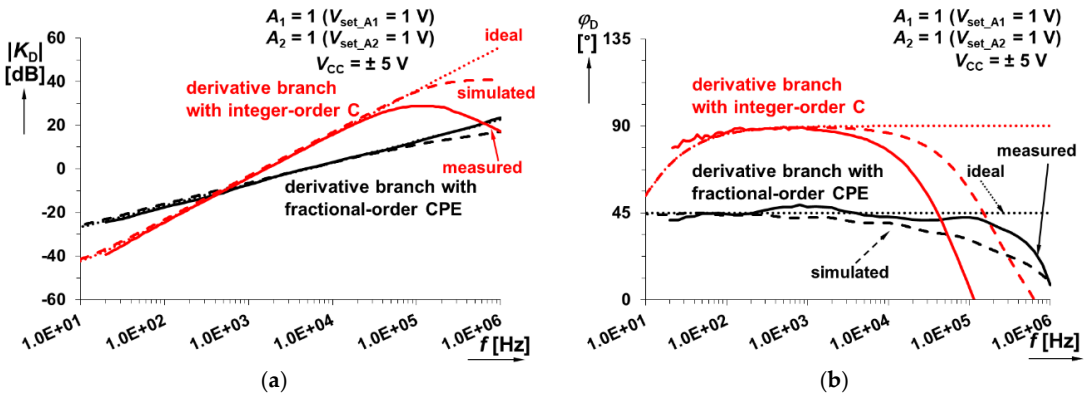


Figure 14. Frequency response of integer-order and fractional-order differentiator: (**a**) magnitude responses; (**b**) phase responses.

6.2. Analysis of Sum of Integer and Fractional-Order Integrator Responses

The experimental setup for this system shown in Figure 3 (both branches are integrators) is analyzed in this subsection. We separated results for the variation of individual scaling gains A_1 and A_2 (0.5→5) to Figures 15 and 16. While one gain was changed, the other one was set to a constant value of 1.

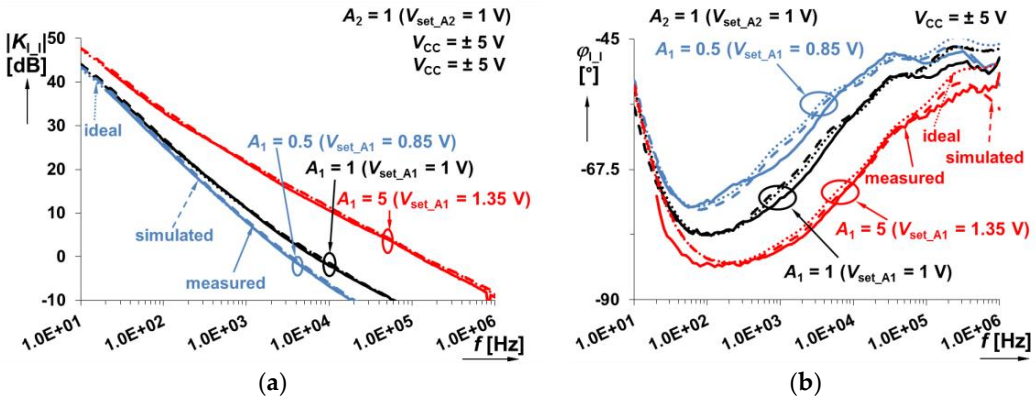


Figure 15. Frequency response of the system shown in Figure 3 (sum of integer- and fractional-order integrator responses) when A_1 (integer-order branch) is varying between 0.5 and 5: (**a**) magnitude responses; (**b**) phase responses.

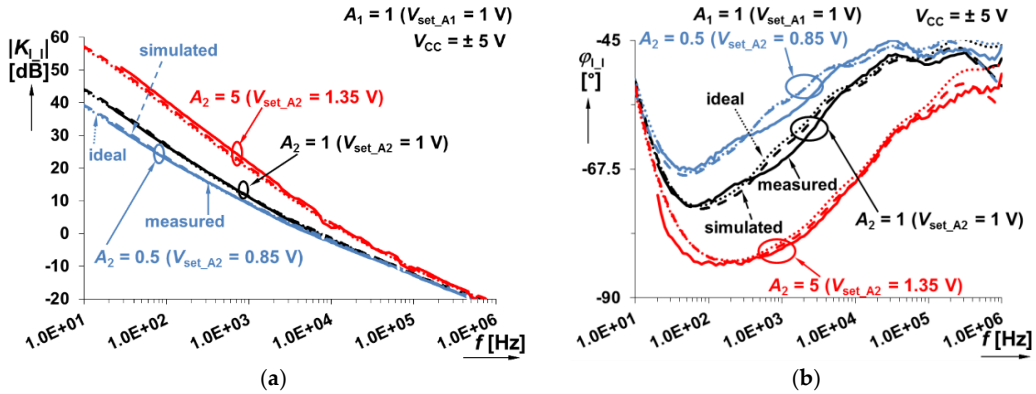
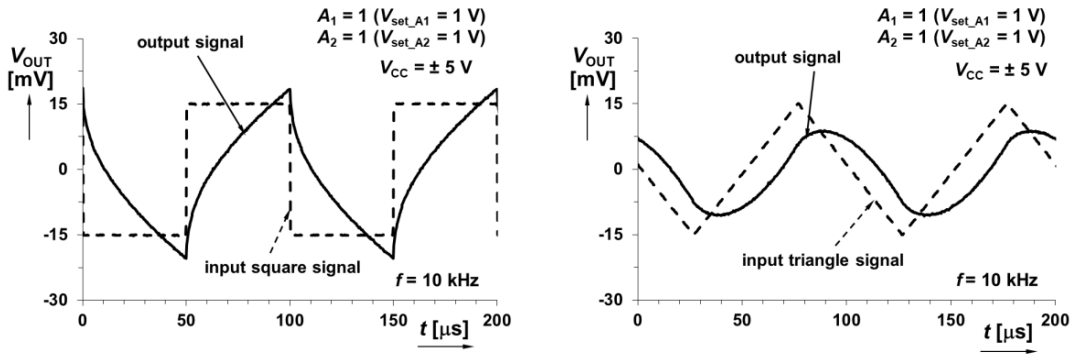


Figure 16. Frequency response of system in Figure 3 (sum of integer- and fractional-order integrator responses) when A_2 (fractional-order branch) is varying between 0.5 and 5: (**a**) magnitude responses; (**b**) phase responses.

The measured time domain responses were studied in more detail at frequency in the middle of the considered band (10 kHz). Output responses on square-wave as well as triangular input voltage are shown in Figure 17 for $A_1 = A_2 = 1$.

The change of gains A_1, A_2 allows one to set time constants of both paths independently (theoretically: $\tau_1 \in$ (200 µs, 20 µs) and $\tau_2 \in$ (11 ms, 1.1 ms) for $A_{1,2} \in$ (0.5, 5.0)) and therefore also the frequency position of the point of break can be electronically controlled. It can be useful for controllers requiring immediate change on their response.

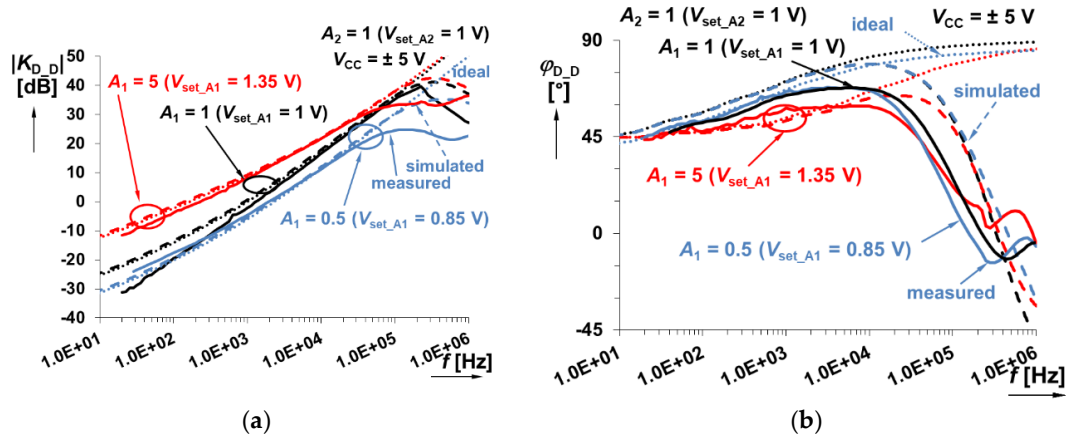


(**a**) (**b**)

Figure 17. Time domain response of system in Figure 3 (sum of integer- and fractional-order integrator responses) when sourced by: (**a**) square wave input signal; (**b**) triangular wave input signal.

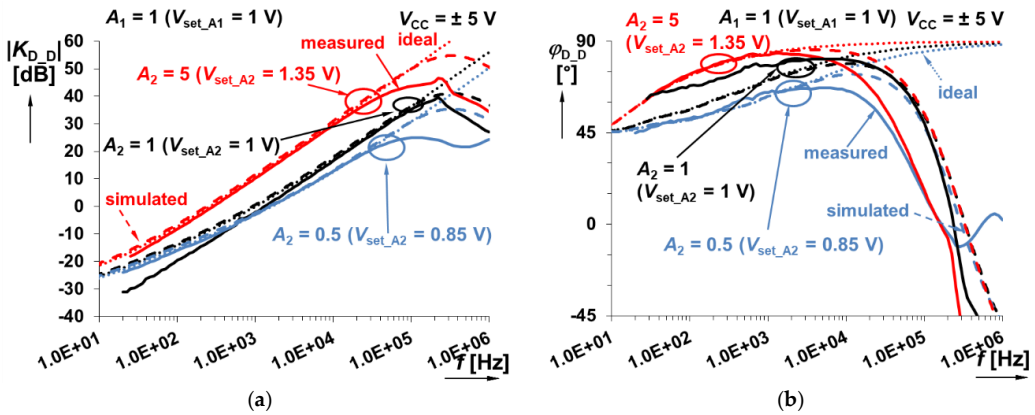
6.3. Analysis of Sum of Integer and Fractional-Order Differentiator Responses

This system shown in Figure 5 consists of differentiators in both branches. The achieved behavior is indicated in Figures 18 and 19 (again for the same values of $A_{1,2}$ gains). Example of time domain analysis of the output response is shown in Figure 20.



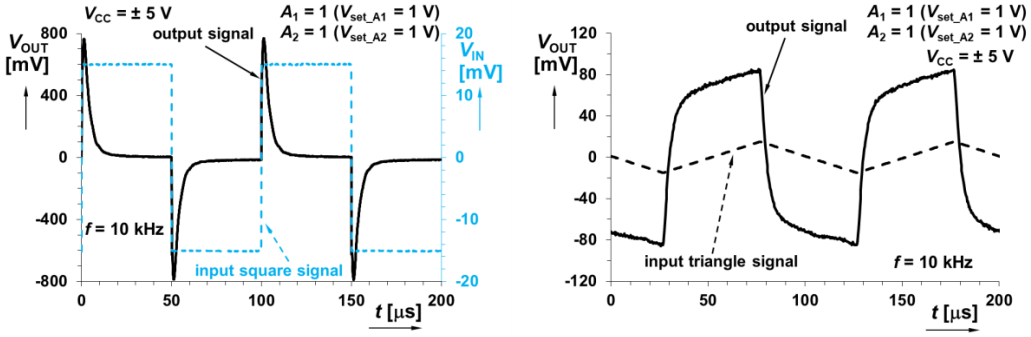
(**a**) (**b**)

Figure 18. Frequency response of the system shown in Figure 5 (sum of integer- and fractional-order differentiator responses) when A_1 (integer-order branch) is varying between 0.5 and 5: (**a**) magnitude responses; (**b**) phase responses.



(**a**) (**b**)

Figure 19. Frequency response of this system shown in Figure 5 (sum of integer- and fractional-order differentiator responses) when A_2 (fractional-order branch) is varying between 0.5 and 5: (**a**) magnitude responses; (**b**) phase responses.

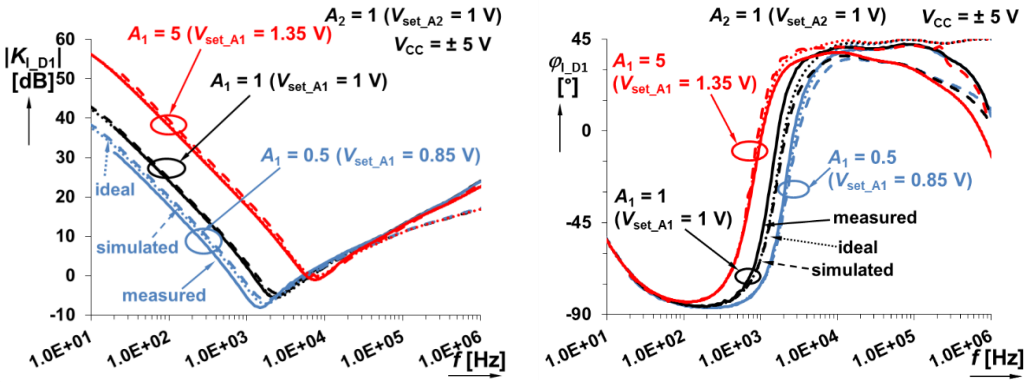


(**a**) (**b**)

Figure 20. Time domain response of the system in Figure 5 (sum of integer- and fractional-order differentiator responses) when sourced by: (**a**) square wave input signal; (**b**) triangular wave input signal.

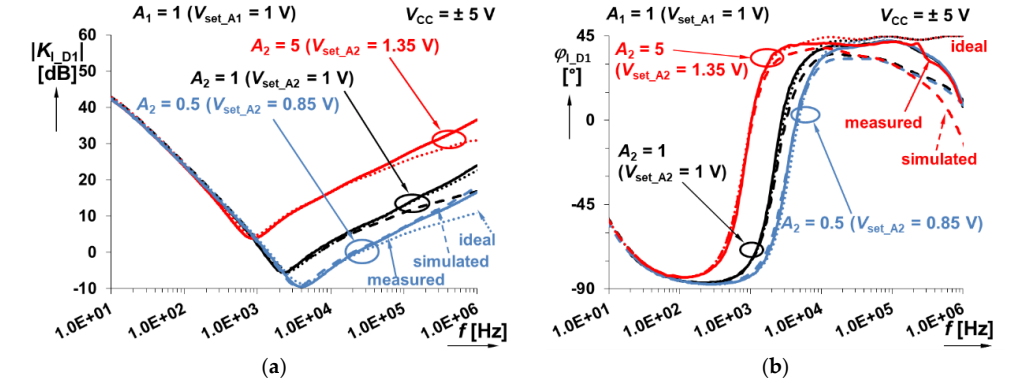
6.4. Analysis of Sum of Integer-Order Integrator and Fractional-Order Differentiator Responses

This specific case shown in Figure 7 implements the sum of integer-order integrator and fractional-order differentiator. Figures 21 and 22 indicate expected minimum of transfer (magnitude) given by intentional zero frequencies. Figures 23–25 show particular time-domain wave forms at frequencies in area with dominance of integration (800 Hz), differentiation (100 kHz), as well as a frequency of 7 kHz being close to the gain minimum (selected example for $A_1 = 5$, $A_2 = 1$).



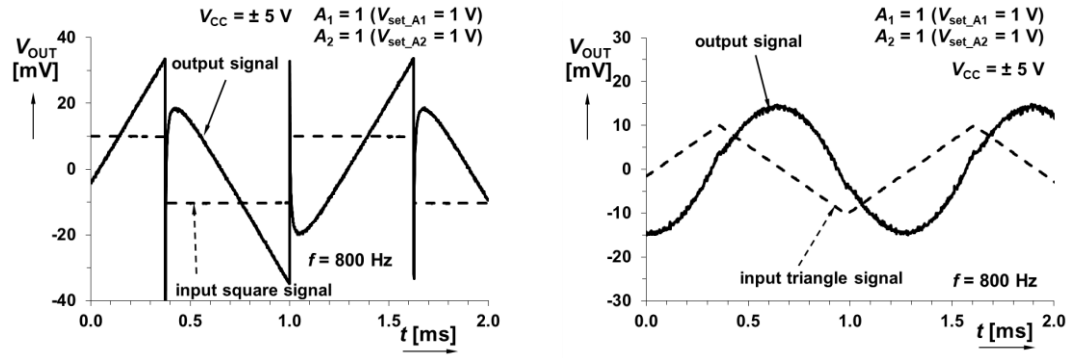
(**a**) (**b**)

Figure 21. Frequency response of the system shown in Figure 7 (sum of integer-order integrator and fractional-order differentiator responses) when A_1 (integer-order branch) is varying between 0.5 and 5: (**a**) magnitude responses; (**b**) phase responses.



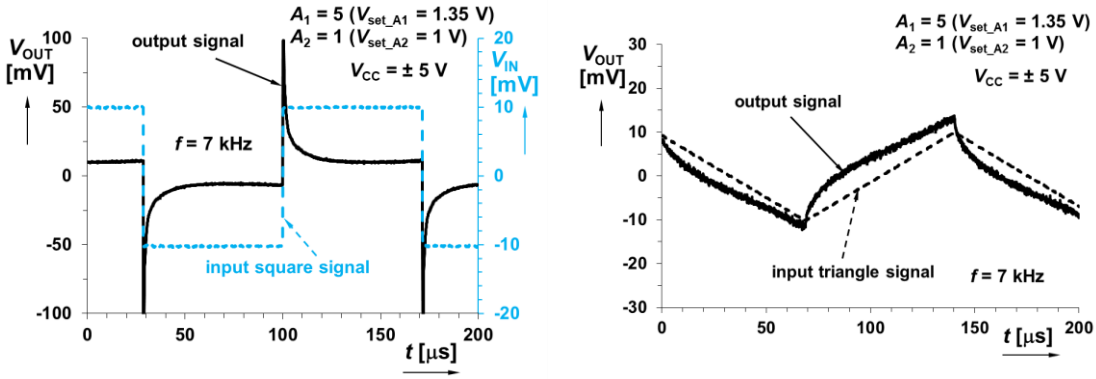
(**a**) (**b**)

Figure 22. Frequency response of the system shown in Figure 7 (sum of integer-order integrator and fractional-order differentiator responses) when A_2 (fractional-order branch) is varying between 0.5 and 5: (**a**) magnitude responses; (**b**) phase responses.



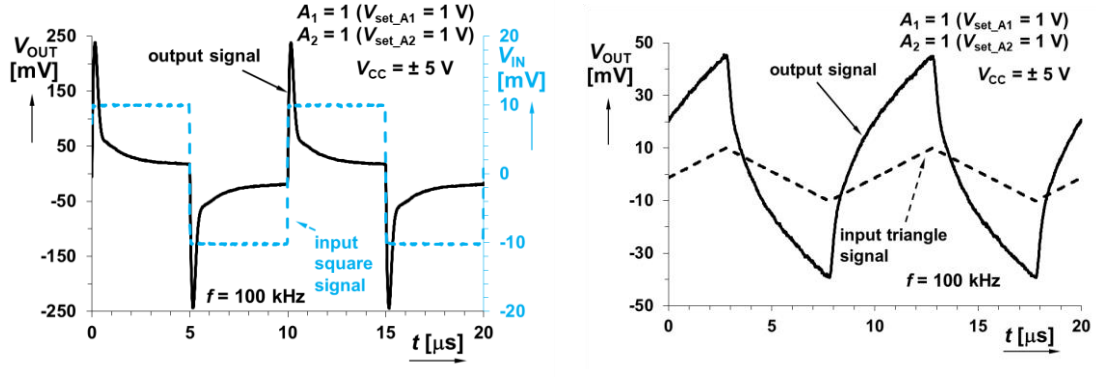
(**a**) (**b**)

Figure 23. Time domain response of the system shown in Figure 7 (sum of integer-order integrator and fractional-order differentiator responses) at 800 Hz when sourced by: (**a**) square wave input signal; (**b**) triangular wave input signal.



(**a**) (**b**)

Figure 24. Time domain response of the system shown in Figure 7 (sum of integer-order integrator and fractional-order differentiator responses) at 7 kHz when sourced by: (**a**) square wave input signal; (**b**) triangular wave input signal.

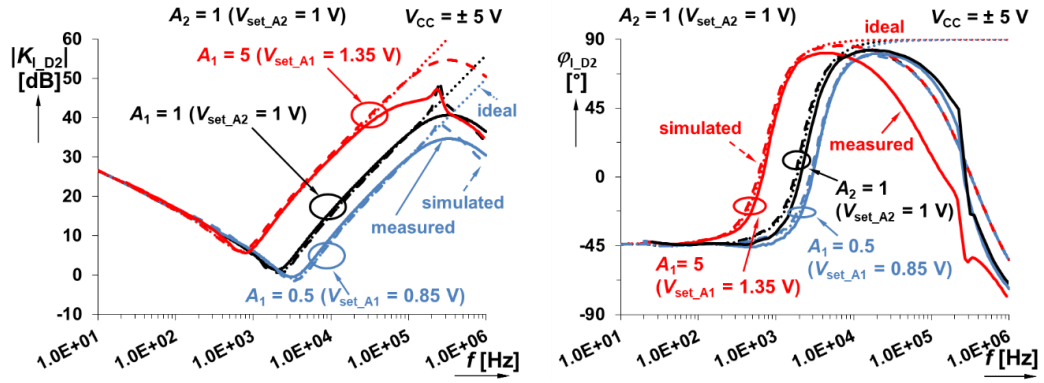


(**a**) (**b**)

Figure 25. Time domain response of the system shown in Figure 7 (sum of integer-order integrator and fractional-order differentiator responses) at 100 kHz when sourced by: (**a**) square wave input signal; (**b**) triangular wave input signal.

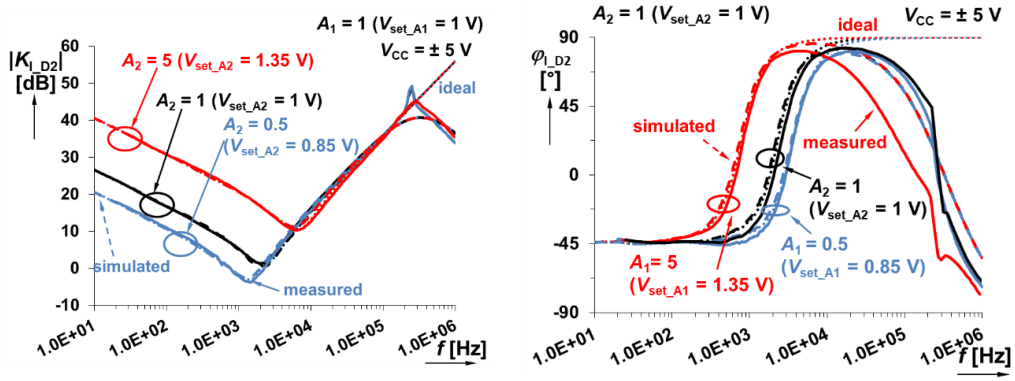
6.5. Analysis of Sum of Fractional-Order Integrator and Integer-Order Differentiator Responses

The last combination of interconnection shown in Figure 9 (sum of fractional-order integrator and integer-order differentiator) was also analyzed, and frequency responses are provided in Figures 26 and 27. Time domain analysis focuses on results obtained at three different frequencies similarly to the previous case (at 600 Hz in the range influenced by fractional-order behavior, at 2.15 kHz at the minimal gain visible for the selected gain setting $A_1 = A_2 = 1$, and for 50 kHz in the derivative area). Results are shown in Figures 28–30.



(**a**) (**b**)

Figure 26. Frequency response of the system shown in Figure 9 (sum of fractional-order integrator and integer-order differentiator responses) when A_1 (integer-order branch) is varying between 0.5 and 5: (**a**) magnitude responses; (**b**) phase responses.



(**a**) (**b**)

Figure 27. Frequency response of the system shown in Figure 9 (sum of fractional-order integrator and integer-order differentiator responses) when A_2 (fractional-order branch) is varying between 0.5 and 5: (**a**) magnitude responses; (**b**) phase responses.

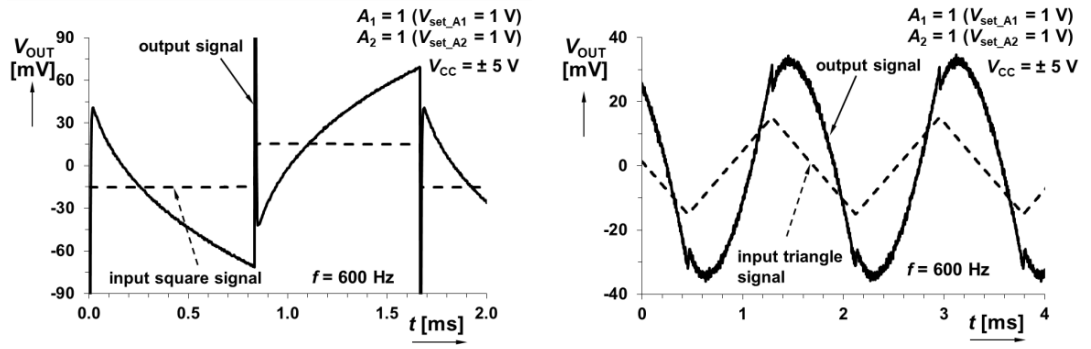


Figure 28. Time domain response of the system in Figure 9 (sum of fractional-order integrator and integer-order differentiator responses) at 600 Hz on: (**a**) square wave input signal; (**b**) triangular wave input signal.

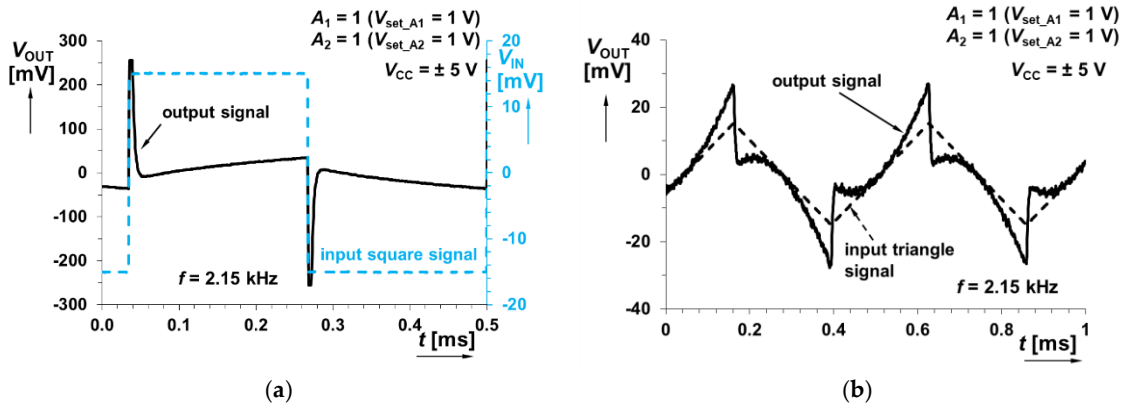


Figure 29. Time domain response of the system in Figure 9 (sum of fractional-order integrator and integer-order differentiator responses) at 2.15 kHz on: (**a**) square wave input signal; (**b**) triangular wave input signal.

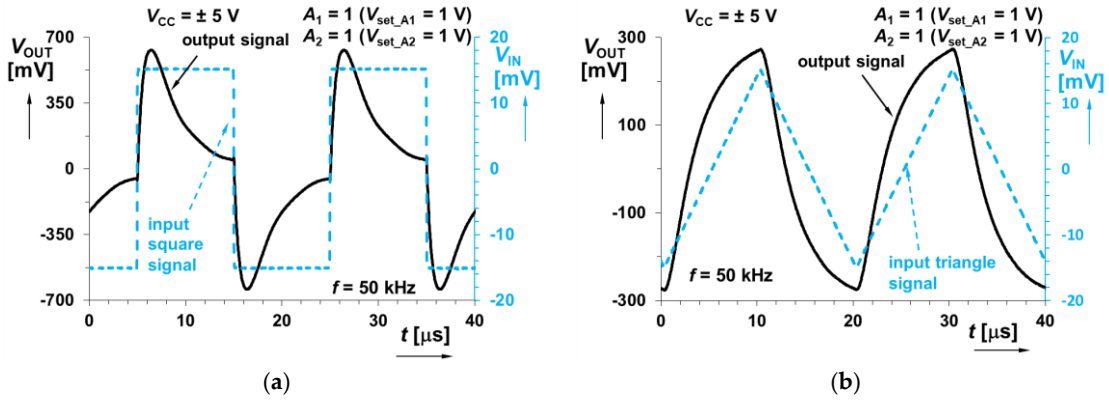


Figure 30. Time domain response of the system in Figure 9 (sum of fractional-order integrator and integer-order differentiator responses) at 50 kHz on: (**a**) square wave input signal; (**b**) triangular wave input signal.

Results presented in this section (Section 6) indicate quite good correspondence of theoretical expectations and experiments. However, high-frequency limitations of active devices as well as other small-signal parasitics influence the high-frequency band significantly. The substantial resonant peak occurs at a frequency around 200–300 kHz. Generally, the frequency limits also depend upon the accuracy of CPE, and therefore, also on used approximation. However, in our case, active devices and real circuitry has significantly higher impact. The resulting operational bandwidth of discussed

systems can be determined between 50 Hz and 100 kHz for both branches, using integrators (fractional and integer-order), between 50 Hz and 10 kHz for both branches, including differentiators, between 50 Hz and 10 kHz for the sum of integer-order integrator and fractional-order differentiator, and finally between 50 Hz and 10 kHz for the sum of fractional-order integrator and integer-order differentiator. The signal dynamics overcomes 40 dB in all presented tests. Therefore, large gain variation occurs, and signals reach very low (tens of mV), as well as very high values (hundreds of mV). It should be considered carefully in the design.

We evaluated selected results of magnitude and phase frequency response (Figure 22) for interconnection in Figure 7 (Section 4.3). The evaluation of simulated and measured frequency responses in the selected case (integer-order integrator and fractional-order differentiator) yields a maximal difference of magnitude of 7 dB in the tested band (10 Hz–1 MHz) and 1.1 dB in the expected (precise) operational range (50 Hz–10 kHz). The deviation 7 dB means the largest magnitude error is about 40% (at high frequencies above 500 kHz) between measured and simulated traces. However, the error is below 12% in the operational band (up to 10 kHz). Note that the relative error (%) seems to be large (tens of %) for small values of gain in units of dB, but the absolute error is acceptable. The phase difference reaches 11° maximally (10 Hz–1 MHz) and 4° (around 10% error) in the suggested operational band (50 Hz–10 kHz). The very similar behavior of all responses indicates that very similar differences are valid also for other cases (magnitude differences between 1–2 dB and phase differences up to 10–15° in the range between 50 Hz and 10 kHz, and higher phase differences especially for integer-order differentiator, as shown in Figure 14).

The results indicate that the specific position of the fractional-order device, as well as the particular combination of two-ports influences slope (point of break in the case of two integrators or two differentiators in resulting topology), or creates a global minimum (combination of integrator and differentiator in resulting topology) and an initial or final phase value in the operational band. Electronic adjustment of transfer responses (gains A_1, A_2) in both paths may be useful for special control applications where the position of global minimum (or point of break) should be impacted immediately in order to optimize effectiveness of regulation during the operation.

Table 2 summarizes the results of maximally achievable magnitude slopes and phase shifts for a theoretical variation of the α parameter and typical experimental results for our case $\alpha = 0.5$ tested in detail. Presented solutions divide the frequency characteristic to two sub-bands (low-frequency and high-frequency—below and above the point of break or global minimum). The fractional-order two-port has a capability to set the initial or final phase shift as well as the slope of magnitude in a specified sub-band arbitrarily in dependence on the α value. The best accuracy with theory was obtained for solutions in Figures 7 and 9. Solutions in Figures 3 and 5 reflect the imperfections and effects of real active devices at high frequencies and the initial behavior of RC approximant at low frequencies, all due to very high processed dynamics in the observed bandwidth.

Table 2. Summarization of theoretical features and experimentally obtained results for studied case (α = 0.5).

	Theoretically Achievable Behavior for Variation of α		**Tested for α = 0.5 ($A_1 = A_2 = 1$)**				
Solution	**Magnitude Slope/Phase Shift (low Frequency Sub-Band)**	**Magnitude Slope/Phase Shift (High Frequency Sub-Band)**	**ExperimentallyEstimated Operational Range (Frequency Bandwidth)**	**Magnitude Slope/Phase Shift (High Frequency Sub-Band)**	**Magnitude Slope/Phase Shift (High Frequency Sub-Band)**	**Experimentally Estimated Dynamics Dependent on $A_{1,2}$ Setting**	**Instability Compensation**
Figure 3	−20 dB/dec −90°	−20·α dB/dec −α·90°	50 Hz–100 kHz	−17 dB/dec −78°	−10 dB/dec -49°	>50 dB	No
Figure 5	20·α dB/dec α·90°	20 dB/dec 90°	50 Hz–10 kHz	16 dB/dec 45°	19 dB/dec 80°	>60 dB	Integer-order integrator
Figure 7	−20 dB/dec −90°	20·α dB/dec α·90°	50 Hz–10 kHz	−20 dB/dec −88°	10 dB/dec +42°	>45 dB	Fractional-order differentiator
Figure 9	−20·α dB/dec −α·90°	20 dB/dec 90°	50 Hz – 10 kHz	−10 dB/dec −45°	21 dB/dec 85°	>45 dB	Integer-order differentiator

7. Conclusions

Four experimentally tested cases of interconnections summing the fractional- and integer-order differentiators and integrators brought interesting results. General operationability of the concepts is limited by the real features of active devices used. The most significant impact has DC accuracy and variable DC offset dependent on the actual setting of gain in the frame of the VGA as well as high-frequency parasitic poles occurring for high gains (differentiator operation). We can state that the proposed concept is approximately operable from 50 Hz up to 10 kHz in all cases.

The gain changes reached more than 45 dB in the observed frequency band (amplification/attenuation of more than 170 times). Therefore, very careful selection of testing input voltage levels is required. The input excitation should be selected in dependence on a particular type of interconnection, but still in range of low tens of mV (30 mV_{P-P} used in tests). However, in specific cases, the input level can reach higher values (hundreds of mV) when operation with low dynamics in limited bandwidths of specific transfer responses (and configurations) is supposed. The expected slopes of experimentally obtained magnitude responses have differences between 1–4 dB/dec from an ideal case in the observed operational bandwidth (50 Hz–10 kHz). The phase responses achieves good results for lower corner phase shifts (45°), where differences from this ideal case are about 3–4° maximally. However, larger phase values at a high-frequency corner for integer-order differentiator are significantly influenced (differences of 10–12° from ideal value) by the frequency limitations of real circuitry (parasitic poles and zeros). The expected maximal differences of measured and simulated traces of frequency responses (in suggested operational bandwidth: 50 Hz–10 kHz) reaches 1–2 dB in magnitude and up to 10–15° (especially at high frequencies due to parasitic behavior of real circuitry). Adjustability of gains in both paths allows influence on the shape of the resulting response in dependence on the specific character of each path (integrator/differentiator) because of their impact on a local minimum or breakpoint. The initial and final phase response can be influenced by the selected α order. Experimental verifications confirmed the expected behavior of the systems quite precisely and obtained results have good correspondence with both simulations and theory. Presented analyses are useful for further applications of studied systems, for example in the design of proportional, integral and derivative controllers or special cases of signal processing requiring these types of transfers (decreasing and increasing gains with different slopes).

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C Higher Order Differentiator Block for Synthesis of Controllable Frequency Dependent Element

Objective 1

Outline

Bibliographic Information

O. Domansky, R. Sotner, J. Petrzela, L. Langhammer and T. Dostal, "Higher order differentiator block for synthesis of controllable frequency dependent elements," *2017 27th International Conference Radioelektronika (RADIOELEKTRONIKA)*, 2017, pp. 1-5, doi: 10.1109/RADIOELEK.2017.7937587.

Author's Contribution

The author surveyed related works, co-proposed a new method, designed and performed the analysis, and wrote a significant part of the manuscript. He was also working on the finalization of the whole manuscript, i.e. reviewing, copy-editing, etc. The presented structure of the differentiator is based on electronically controllable current conveyors (ECCIIs), current conveyor of the second generation (CCII) and electronically controllable gain amplifier (VGA). This structure was applied as an example of the 3rd order differentiator and frequency dependent negative resistors (FDNRs) of integer (as well as fractional) order. Results in this paper use a summing block and two paths using independently adjustable voltage gains including two different transfer responses (Objective 1).

Author's contribution: 69 % (the main author).

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(https://ieeexplore.ieee.org/document/7937587/).

Higher Order Differentiator Block for Synthesis of Controllable Frequency Dependent Elements

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***Abstract*— This paper presents structure of generally nth-order differentiator transfer block serving for purpose of integer order or fractional order immittance (impedance) synthesis. Presented structure of the differentiator is based on electronically controllable current conveyors (ECCIIs), current conveyor of second generation (CCII) and electronically controllable gain amplifier (VGA). This structure was applied as example of 3rd order differentiator and frequency dependent negative resistors (FDNRs) of integer (as well as fractional) order. Proposed applications offer electronic controllability of time constant, magnitude value and reconfigurability of impedance character (between positive and negative). PSpice simulations were performed in order to verify presented concepts.**

Keywords—differentiator; constant phase element; current conveyors; electronic control; FDNR; fractional order FDNR; reconfigurability

I. INTRODUCTION

Transfer blocks of integer order higher than 2 are well known in circuit theory of common analog systems. They are called frequency filters of passive or active construction. Their transfer functions are polynomial rational expressions of frequency dependent complex variable s. Denominator always consists of all integer powers of s ($s^0 \ldots s^n$) till the highest power given by order of the function. However, also transfer structures having only the highest power of s in transfer function are very important. They are known as integrators or differentiators ($K_I(s) = k/s$, $K_D = ks$). So-called lossy types of these integrators ($K_I(s) = k/(s+k)$, $K_D(s) = s/(s+k)$) are also known as simple first-order low-pass and high-pass filters [1], [2]. These subparts are very important for many analog systems. The functions having character of polynomial description but expressed as impedance or admittance are known as lossless or lossy inductances or capacitances. Transformation from transfer function to immittance function is quite simple task (additional voltage to current conversion of the output response fed back to the input high-impedance node [3]). First-(integer)order immittances are very useful and known from the field of so-called synthetic elements [1], replacing inductances by capacitors and proper active circuitry, operating in real systems when required. Second-order immittances in form $Z_C(s) = ks^2$ are known under designation frequency dependent negative resistor (FDNR) [4] and their application field focuses on design of RLC ladder filtering structures. They serve as key subpart in so-called Brutton transformation [4]-[7] in the most cases. The second-order frequency dependent elements are generally called as super-immittances [8].

A cascade of first-order integrators [1] only creates nth-order integrator. However, construction of differentiator is not so easy task. The same idea (cascade of lossless differentiators utilizing grounded capacitors) is not suitable method because of larger complexity of differentiator than integrator [3] (except opamp based concept, however, using floating capacitor and no possibility to immediate electronic control). Multiplication of transfer segments in the feedback loop is a key feature in synthesis of higher order blocks and elements. Discussion of this method should start from circuits known under designation impedance (or immittance) converters and inverters [3], [6] or synthetic elements. The simplest solutions are based on operational transconductance amplifiers (OTAs) [1]-[3]. However, only impedance conversion (from capacity to inductance in most cases) is their main intention. Therefore, further features extending overall immittance function are not explored very often. Paper [9] indicates feasibility of extension of circuitry in order to obtain more complex overall immittance functions. Note that classical well-known Antoniou impedance converter [10] is not so suitable for intended purposes due to limited feasibility of multiplication, quite complex circuity and lack of electronic controllability. Two opamps and five passive elements (four of them are floating) are required for result in form of multiplication of three impedances divided by two impedances. This is not effective for intended purposes (see for example [11]). Therefore better concepts should be studied.

Methods for multiplications and conversions/inversions of immittances of higher order can be beneficially used also in synthesis of fractional order elements also known as constant phase elements (CPEs). Works [12]-[15] introduces solution of CPE based on specific filtering responses created by multiple feedback structure and subsequent voltage to current conversion of output response to high-impedance input of the system. On the other hand, the same result can be achieved by simple voltage to current conversion of the transfer response of bilinear blocks in simple cascade [16] into the input with less complexity in some cases.

Research described in this paper was financed by Czech Ministry of Education in frame of National Sustainability Program under grant LO1401. For research, infrastructure of the SIX Center was used. Research described in the paper was supported by Czech Science Foundation project under No. 15-22712S.

Our paper brings interesting structure serving for generally n^{th}-order differentiator design as well as its simple modification of frequency dependent higher order immittances of inductive character. This structure offers theoretically arbitrary selection of the order by simple modification in the feedback loop (adding or removal of segments). Commercially available elements are selected in order to perform initial verifications of our intentions by PSpice simulations.

II. General Electronically Controllable Higher Order Differentiator Block

Active devices used in following circuits should be described and explained briefly. Electronically controllable current conveyor of second generation (ECCII) [17] is very useful device for synthesis and design of controllable applications. It's ideal definition supposes terminal relations: $V_Y = V_X$, $I_Y = 0$, $I_Z = B \cdot I_X$ and availability of simple control of parameter B (current gain) by DC voltage. Note that B can be positive or negative in dependence of particular type of ECCII (ECCII+/-). Version of current conveyor of second generation having fixed gain $B = \pm 1$ is abbreviated as CCII+/-. These devices will be used in our designs. Specifications of current mode multiplier EL2082 [18] and current feedback operational amplifier (CFOA) AD844 [19] offer implementations of these commercial devices for our purposes.

Generalized structure of the nth-order voltage mode differentiator block is shown in **Fig. 1**. The structure in **Fig. 1** has transfer function in form:

$$K_D(s) = \frac{V_{OUT}}{V_{INP}} = s^n \prod_{i=1}^{n} \frac{C_i R_i}{B_i}, \qquad (1)$$

that can be simplified (considering $R_1 = R_2 = \ldots = R_n = R$, $C_1 = C_2 = \ldots = C_n = C$ and $B_1 = B_2 = \ldots = B_n = B$) into:

$$K_D(s) = \left(\frac{sCR}{B} \right)^n. \qquad (2)$$

Note that full implementation of the block (**Fig. 1**) in voltage mode requires additional voltage buffer at input terminal (connected to R_X) to increase input impedance given directly by R_X in **Fig. 1**. However, additional utilization of unity gain buffers depends on specific implementation where discussed blocks will be applied.

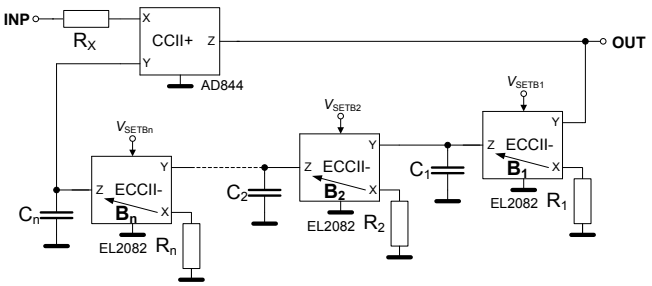

Fig. 1. Generalized structure for synthesis of nth-order differentiator.

III. Examples of Application

Proposed structure can be useful in transfer blocks as well as in immittance (impedance or admittance) emulators after certain modification. Values of active and passive parameters were selected as follows: $R_X = 1\ \text{k}\Omega$ ($950 + 50\ \Omega$ internal resistance of X terminal of AD844 [19]), $R_1 = R_2 = R = 560\ \Omega$ ($470 + 95\ \Omega$ internal resistance of X terminal of EL2082 [18]), $C_1 = C_2 = C_3$ (where applicable) $= C = 10$ nF, initial $B_1 = B_2 = B = 1$ (all $V_{SETB} = 1$ V). All result were performed by PSpice simulations with $V_{DD} = \pm 5$ V.

A. 3rd-order differentiator

Design of the circuit from **Fig. 1** was provided for $n = 3$ in accordance to all above stated parameters. The particular transfer function has form:

$$K_D(s) = \left(\frac{sCR}{B} \right)^3. \qquad (3)$$

Results of simulation are given in **Fig. 2** where trace slope +60 dB/dec was obtained as expected.

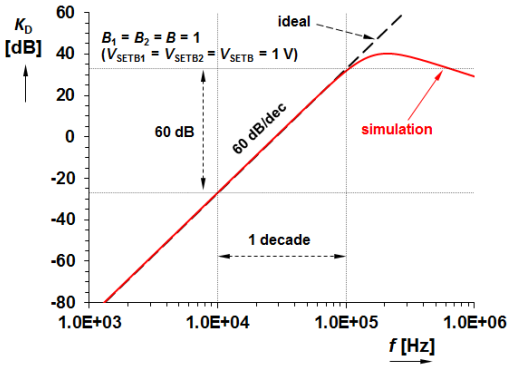

Fig. 2. Magnitude transfer response of 3rd-order differentiator from Fig. 1.

B. Integer order eletronically tunable negative/positive frequency dependent resistor

Simple modification of the structure from **Fig. 1** offers construction of electronically tunable frequency dependent negative resistor of the second-order as shown in **Fig. 3**. This circuit may operate also as positive frequency dependent element due to availability of reconfiguration of polarity by amplitude gain A of the voltage mode variable gain amplifier (VGA). This modification supposes external R_X polarity change by VGA (where $A = 10^{2(|V_{SETA}|-1)}$ for VCA610 type [20]). Note that V_{SETA} is physically connected with negative polarity. Overall impedance is defined as:

$$Z_C(s) = \frac{V_{INP}}{I_{INP}} = s^2 D = s^2 \left(\frac{CR}{B} \right)^2 \frac{R_X}{1 - A}. \qquad (4)$$

where $A = 0$ ($V_{SETA} = 0$ V) performs positive frequency dependent resistor and $A = 2$ ($V_{SETA} = 1.15$ V) reconfigure structure in **Fig. 3** to FDNR. Ideal value for $B_1 = B_2 = B = 1$ ($V_{SETB} = 1$ V) is given as $D = |Z_C(f)|/(2\pi f)^2 = 31.4 \cdot 10^{-9}\ \Omega^3\text{F}^2$. Results confirming intended behavior are shown in **Fig. 4** (figures include important parameters and notes). Simulations yield $D = 32.2 \cdot 10^{-9}\ \Omega^3\text{F}^2$ for $A = 0$ and $29.6 \cdot 10^{-9}\ \Omega^3\text{F}^2$ for $A = 2$.

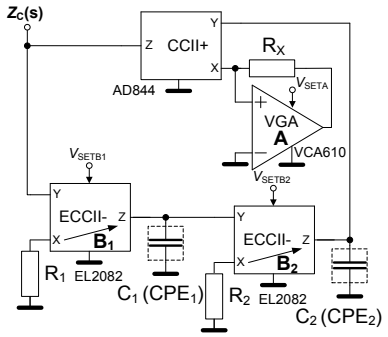

Fig. 3. Electronically tunable frequency dependent positive/negative resistor created from structure in Fig. 1.

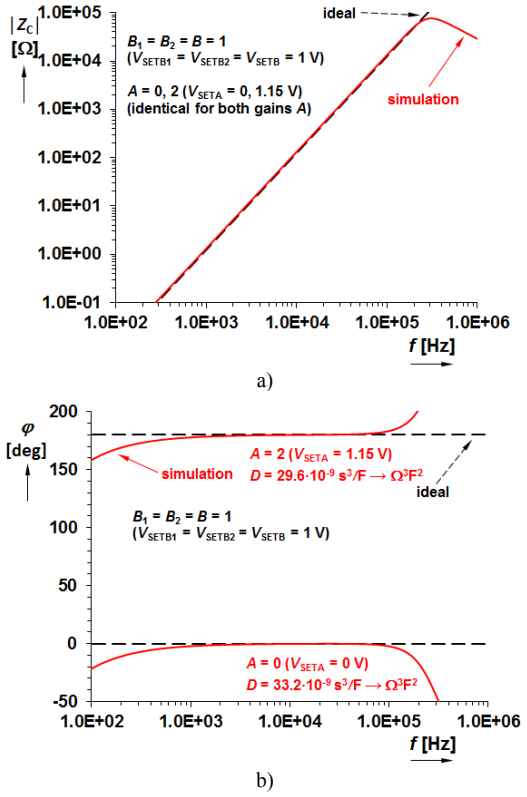

Fig. 4. Impedance characteristic of circuit in Fig. 3 for both configurations (positive and negative): a) magnitude responses, b) phase responses.

Real input resistance in input node (R_p) causes high-frequency limitation in simulated responses (parasitic pair of complex conjugated poles) at frequency:

$$f_p = \frac{1}{2\pi RC}\sqrt{\frac{(1-A)R_pB^2}{R_X}}, \qquad (5)$$

as it can be clearly visible in **Fig. 4** and **Fig. 6**. This pole frequency is dependent on tuning process (adjusting of B), therefore, it cannot be avoided in real case. Significantly high real part of input resistance can only suppress this effect and move this pole to higher frequencies.

C. *Fractional order FDNR*

Synthesis of passive versions of constant phase element (CPE) with inductive character is not easy task because such a design requires presence of real inductances (coils) in the structure (RL segments) [21], [22]. Therefore, design of fractional order active FDNR with CPEs ($Z_{CPE}(s) = 1/(s^\alpha C_\alpha)$) of capacitive character (fractional order capacitances) and subsequent impedance conversion seems to be better approach. Structure presented in **Fig. 3** offers interesting performance also for fractional order circuits. Such modification requires only simple replacement of integer order capacitors by fractional order capacitors (CPEs with capacitive character) in **Fig. 3**. Then the overall impedance has form:

$$Z_C(s) = \frac{V_{INP}}{I_{INP}} = s^{\alpha+\beta}\left(\frac{C_\alpha R_1}{B_1}\right)\left(\frac{C_\beta R_2}{B_2}\right)\frac{R_X}{1-A}, \qquad (6)$$

that could be simplified when $R_1 = R_2 = R$ and $C_\alpha = C_\beta$, $B_1 = B_2 = B$ into:

$$Z_C(s) = s^{2\alpha}D_\alpha = s^{2\alpha}\left(\frac{C_\alpha R}{B}\right)^2\frac{R_X}{1-A} \qquad (7)$$

where $C_\alpha = 1/X_{CPE\alpha}$ and identical order ($\alpha = \beta$) of both CPEs is supposed. Design method and calculations explained in [21], [22] were used for design of fractional order CPEs with capacitive character (containing RC segments only). Parameters of CPE structure are shown in **Fig. 5** for $\alpha = 1/3$, $X_{CPE\alpha} = 10$ kΩ (phase shift of $Z_C(s)$ of FDNR $\varphi = 90\cdot 2\alpha = 60$ degree). Results of simulation as well as tuning process (available also in all previous cases) are shown in **Fig. 6**. We are supposing $A = 2$ ($V_{SETA} = 1.15$ V) and $B_1 = B_2 = B$ ($V_{SETB1} = V_{SET2B} = V_{SETB}$) set to 0.1, 0.5, 1.0, 2.0 V for adjusting of D_α.

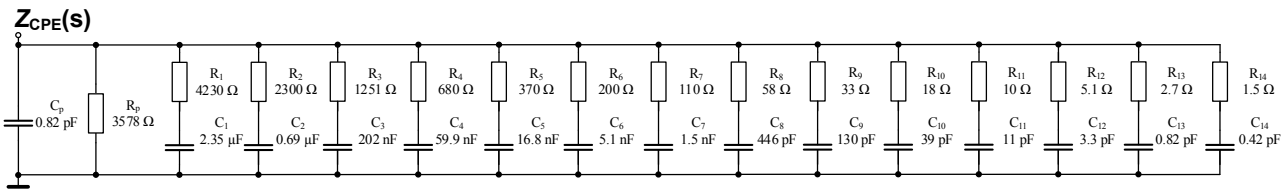

Fig. 5. Constant phase element (and its values) for implementation in Fig. 3 instead of integer order capacitors.

IV. Conclusion

Proposed structure of the nth-order differentiator in **Fig. 1** was tested in three different applications (3rd-order differentiator, frequency dependent negative/positive resistor of the second order, and fractional order FDNR with inductive character utilizing fractional order capacitors (CPEs) of identical order $\alpha = 1/3$). Electronic control of the time constant as well as impedance magnitude or polarity (positive/negative) is possible through adjustable parameters of the structure (current and voltage gains). The main benefits of this concept are: a) simple extension of any order of the transfer response (differentiator) or immittance (frequency dependent negative/positive resistor), b) electronic controllability, c) always grounded capacitors, d) suitability for integer as well as fractional order synthesis. These features were verified by PSpice simulations and obtained results are in good agreement with theoretical intentions.

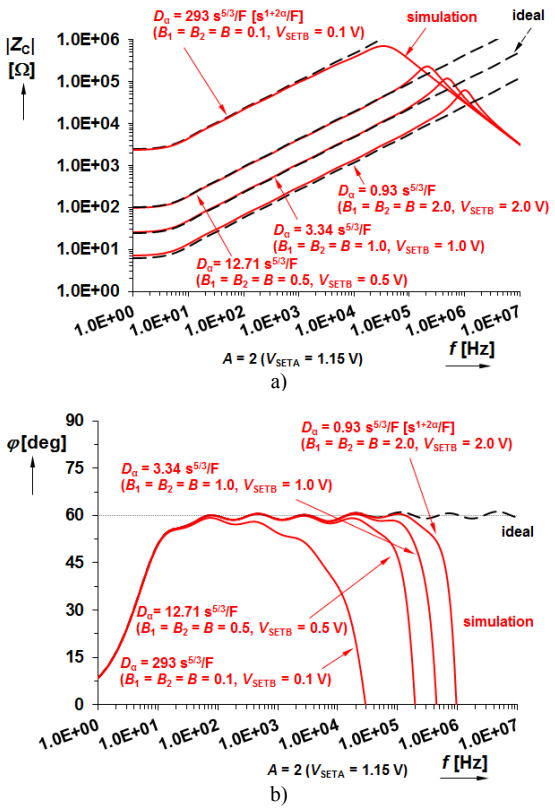

Fig. 6. Impedance characteristic of circuit in Fig. 3 for fractional order capacitors with $\alpha = 1/3$ at positions C_1 and C_2: a) magnitude responses, b) phase responses.

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D Reconfigurable Impedance Converter for Synthesis of Integer and Fractional-Order Synthetic Elements

Objective 2

Outline

Bibliographic Information

O. Domansky, R. Sotner and L. Langhammer, "Reconfigurable Impedance Converter for Synthesis of Integer and Fractional-Order Synthetic Elements," *2018 41st International Conference on Telecommunications and Signal Processing* (*TSP*), Athens, Greece, 2018, pp. 1-5, doi: 10.1109/TSP.2018.8441376.

Author's Contribution

The main authorship took part in designing an experimental setup, data measurements and processing, visualization, and contributions to the whole manuscript.

This paper presents design and study of difference between the integer and fractional-order impedance (synthetic inductor) allowing the impedance magnitude adjustment (inductance value adjustment). The adjustment of equivalent inductance is provided by single current gain (controlled by DC voltage) and adjustment (or minimization) of serial losses by the second adjustable current gain parameter. It is crucial to alter parameters (ideally DC voltage) of the final network structure without having to modify the internal configuration of the circuit. This paper presents and addresses this issue. Therefore, presented topology fulfills the intended target of Objective 2 regarding standard solutions in literature.

Author's contribution: 70 % (the main author).

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(https://ieeexplore.ieee.org/document/8441376/).

Reconfigurable Impedance Converter for Synthesis of Integer and Fractional-Order Synthetic Elements

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***Abstract*— This paper introduces a practical and straightforward view on the design of circuit based on electronically controllable current conveyors (ECCIIs), wide-band operational transconductance amplifier (OTA), differential difference amplifier (DDA) implemented as voltage buffer (BUF) and four quadrant current-mode multiplier. All these elements are implemented for the possibility of multiple electronical tunability (via DC voltage parameter V_{SET}) of the resulting specific reconfigurable impedance converter of the integer-order as well as the fractional-order. This solution leads to circuit with electronically controllable input impedance (lossy/lossless character with additional fractional-order element). In addition, a constant phase element (CPE) is tested in order to maintain a constant phase response (depending on which phase change is realized) and phase ripple in a specific frequency band. All theoretical assumptions are supported by PSpice simulations.**

Keywords—current conveyors, electronically tunability, constant phase element, synthetic element, input impedance

I. INTRODUCTION

In recent years, the active elements attract increasing attention due to the possibility of an electronic tunability. It seems to be very important to change some parameters of the final network structure without the needs to change the internal layout of the circuit itself. Commonly used active devices are electronically controllable current conveyors of the second-generation [1]. Nowadays, the current conveyors are widely used for their beneficial behavior in current (CM) [2], voltage (VM) [3] or mixed mode (MM) circuits [1]. Those parts could be widely used in various analog signal processing.

The so-called synthetic elements [4] offer the most common usage in the filtering design. The final immittance function of the described elements could be expressed as an impedance/admittance having lossy or lossless [5] capacitive character (decreasing magnitude response with frequency) or an inductive character (increasing magnitude response). However, a circuit design consisting of inductors on chip, could be challenging task and in most of the times it could cause problems. Many solutions are simulated and created using various types of active (operational amplifiers (OA), current conveyors etc. [6]-[7]) and passive elements (resistors and capacitors).

Research described in this paper was financed by National Sustainability Program under grant LO1401. For research, infrastructure of the SIX Center was used. This article was supported by Specific Research under internal grant no. FEKT-S-17-4707.

TABLE I. COMPARISON OF SYNTHETIC ELEMENTS SOLUTION USING DIFFERENT TYPES OF ACTIVE ELEMENTS

	No. of passive elements	No. of active elements	Type of active elements	All capacitors grounded	Type of control	No. of decades of valid operation	Fractional-order solution
[8]	5 (8)	2	OPAMP[a]	No	passive only	N/A	No
[9]	6	1	ICCII[a]	No	passive only	2	No
[11]	2 (4)	1	VDCC[a]	Yes	g_m	2.5	No
[12]	4	4	ECCII	Yes	DC voltage	3	No
[13]	4	1	CFOA[a]	Yes	passive only	3.5	No
[15]	2	1	VDCC[a]	Yes	control current	2.5	No
[17]	4	2	CFOA[a]	Yes	passive only	2	Yes
proposed structure							
	3	4 (5)	ECCII	Yes	DC voltage	4	Yes

[a] OPAMP – operational amplifier, ICCII - inverting current conveyor of the second generation, VDCC - voltage differential current conveyor, CFOA - current feedback operational amplifier

The so-called Antoniou [8] and Riordan [5] impedance converter are the best-known synthetic structures representing advanced immittances (inductances, frequency dependent negative resistors, for example). Unfortunately, both of the mentioned network solutions ([5], [8]) are unsuitable for all application purposes because of lack of electronic tunability and a large amount of components (two OAs and five passive impedances where four of them are not grounded). Therefore, the designers are looking for the alternative ways how to produce synthetic elements.

In the past decade, many workers contributed to this field of research. Most of them aim to minimize the resulting solution (amount of the elements) needed for synthesis [9]

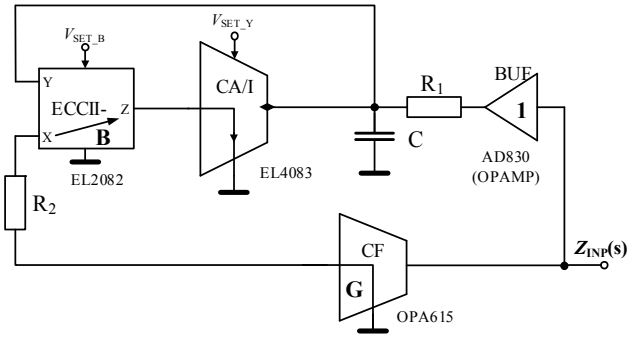

Fig. 1. Synthetic inductor using four active and three passive elements.

(four active and two passive elements for single gyrator) and construction of topologies where all the capacitors are grounded [10] (four current conveyors and seven passive elements). Usage of such circuits can be described as a lossless floating inductance designed with voltage differencing current conveyor [11], a pseudo-differential floating inductance simulator [12] or as an inductance simulators [13] using single controlled gain voltage differencing current conveyor [14]-[15]. A comparison of different solutions based on various active elements can be seen in Table. 1.

Our work brings novelty in term of simplification of the synthetic element (namely the synthetic inductance) and introduces the electronic way of controllability (DC voltage). This paper is divided into several parts particularly Section II deals with a new circuitry of synthetic inductance (Fig. 1). This circuit targets on the minimal amount of elements needed for implementation having required features (four active elements and three passive elements). Section III brings tunability into the circuit by adding one more active element driven by voltage (Fig. 5). And finally, Section IV focuses on the magnitude and the phase changes of the resulting structure by a substitution of the integer-order capacitor by the constant phase element [16]-[20] with $\varphi = 30\,°$ angle (CPE30) [20].

II. Newly Proposed Structure of a Sythetic Inductor with Four Active Elements

The interconnection of the components of the proposed structure (Fig. 1) is quite simple and will be described briefly. The electronically controllable current conveyors of the second generation (ECCIIs) [1] create the key parts of this design. Current gain between terminal X and Z can be electronically controlled via current gain B parameter that is allowed by DC voltage (V_{SET_B}). Several types of these devices (ECCIIs) such as ECCII- with negative polarity of terminal Z, ECCII+ with positive polarity of terminal Z and ECCII+/- maintaining both polarities (Z+ and Z-) has been defined in literature [1]. The ideal definition of current conveyor can be expressed by its inter-terminal features (voltages and currents): $I_Y = 0; V_x = V_Y$ and $I_Z = B \cdot I_x$ where B represents the current gain proportional to DC control voltage (V_{gain}) [21].

EL2082 (a specification can be found in [21]) there have been four intended purposes selected with feedback loop from port Z to Y (to node of R_1, C). Differential difference

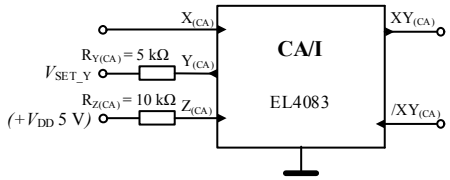

Fig. 2. Block scheme of CA/I mentioned in Fig. 1.

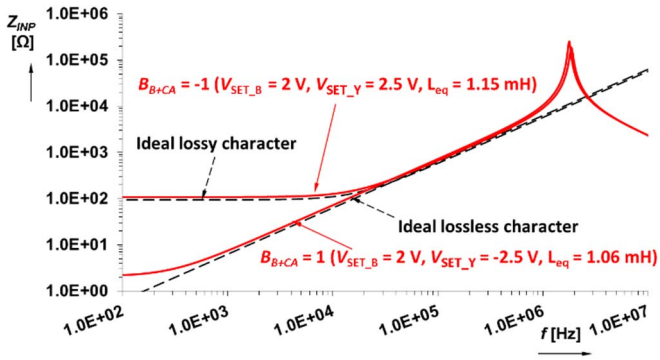

Fig. 3. Lossy/lossless magnitude input impedance characteristic of the scheme in Fig. 1 in dependence of setting parameter B_{B+CA} = 1 and B_{B+CA} = -1.

amplifier (DDA) AD830 [22] connected as the voltage buffer ($V_{OUT} = V_{INP}$) (having gain of A = 1) is required in the loop (also every other operational amplifier connected as the buffer would be sufficient). Port X is connected through R_2 to OPA615 [23] in configuration of the common base current amplifier (with the low input impedance). The ECCII- with V_{SET_B} is subsequently complemented by the current amplifier (CA) based on four-quadrant current-mode multiplier EL4083 [24].

Output current of CA/I can be expressed as: equals $I_{XY} = I_X I_Y (2I_Z)^{-1}$. Terminal $Y_{(CA)}$ of the EL4083 is driven by DC voltage V_{SET_Y}. It offers the possibility of polarity inversion of the parameter B. In this particular case a new current gain parameter is needed (B_{B+CA}) in order to maintain usable amplification of the output signal. B_{B+CA} is the final product of ECCII- (V_{SET_B}) and CA/I (V_{SET_Y}). Fig. 2 shows a block scheme part mentioned above. There could also be two ICs in the cascade in order to get both polarities of the gain (it is not possible to do it with just one of the EL4083).

The overall impedance has the form:

$$Z_{INP}(s) = \frac{V_{INP}}{I_{INP}} = \frac{-R_2 + B_{B+CA} R_1 - s(R_1 C R_2)}{-1}, \quad (1)$$

where gain (A) of BUF is set to 1 as well as gain (G) of OPA615. Regarding previous setting, the overall impedance could be modified to the form of:

$$Z_{INP}(s) = \frac{V_{INP}}{I_{INP}} = R_2 - B_{B+CA} R_1 + s(R_1 C R_2). \quad (2)$$

In order to readjust between the lossy or the lossless impedance character, two parameters are suitable to deliver it.

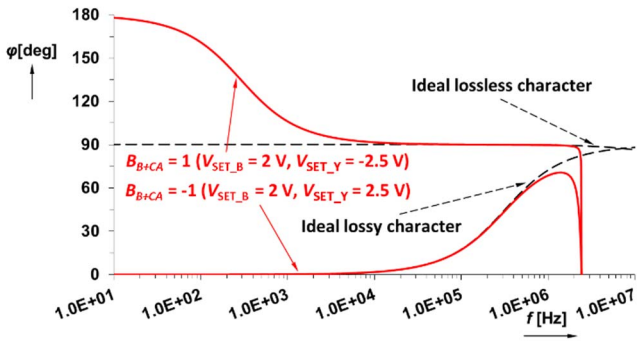

Fig. 4. Phase response characteristic for setting of parameter $B_{B+CA} = 1$ and $B_{B+CA} = 1$.

The first one is V_{SET_B} that sets the parameter B of the ECCII-. Note that when $B_{B+CA} = -1$, the possibility of simplification of the equation (1) for the positive lossy character (B_{B+CA} is set to -1 exists under condition of $R_1 = R_2; R_1 + R_2 = R_{1,2}$):

$$Z_{INP}(s) = R_2 - (-1) \cdot R_1 + s(R_1 C R_2) = R_{1,2} + s(R_1 C R_2). \quad (3)$$

The lossless impedance character is obtained for B_{B+CA} equal to 1, then impedance equation modifies into:

$$Z_{INP}(s) = R_2 - 1 \cdot R_1 + s(R_1 C R_2) = s(R_1 C R_2). \quad (4)$$

The simulations in Fig. 3 and Fig. 4 are performed in Pspice to support of the theoretical expectations. The settings of the parameters are as follows: lossless inductive impedance character, $B_{B+CA} = 1$ ($V_{SET\_B} = 2$ V [21], $V_{SET\_Y} = -2.5$ V [24], $G = 1$, $V_{DD} = 5$ V). For lossy inductive impedance character $B_{B+CA} = -1$ ($V_{SET\_B} = 2$ V, $V_{SET\_Y} = 2.5$ V, $G = 1$).

Regarding the passive values of the passive elements $C = 1$ nF, $R_1 = R_2 = 1$ kΩ = (895 Ω + 95 Ω + 10 Ω) where the additional 95 Ω and 10 Ω are the impedances of OPA615 and EL2082. Simulations results were obtained for the phase shift as well. The same settings as for the magnitude impedance characteristics in Fig. 3 in full frequency range have been used and resulting traces can be seen in Fig. 4. Note that the real input impedance of terminal Z_{INP}(s) causes the parasitic pole at high frequencies and it cannot be avoided in the real measurements.

III. The Additional Extension of Control with Second Current Conveyor.

For the extended control of the solution, the circuit in Fig. 1 can be modified with one additional ECCII- (Fig. 5) connected in collector node of OPA615 (additional current gain parameter B_2). This extension has no effect on the lossy character of the input impedance if $B_2 = 1$ and causes the same results as in Fig. 3 and in Fig. 4. Also the parameter V_{SET_B2}, (B_2) can be set in range of -1 V up to +7 V [21]. In practice, we tested $V_{SET\_B2} = 0.1$ V, $V_{SET\_B2} = 0.4$ V, $V_{SET\_B2} = 1$ V and $V_{SET\_B2} = 4$ V in Fig. 6.

The overall input impedance of the circuit from Fig. 5 achieves expression:

$$Z_{INP}(s) = \frac{V_{INP}}{I_{INP}} = \frac{-R_2 + B_{B1+CA} R_1 - s(R_1 C R_2)}{-1 \cdot B_2}. \quad (5)$$

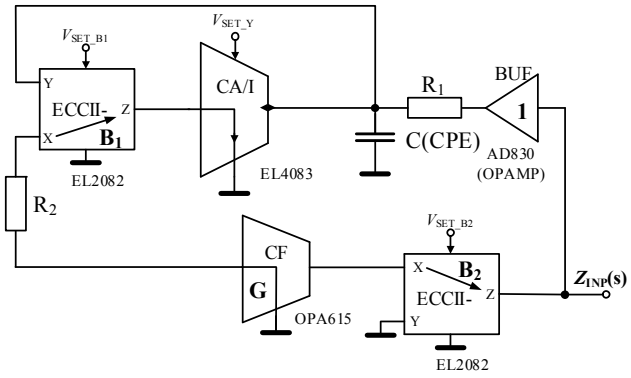

Fig. 5. Extended circuitry of synthetic inductor using five active and three passive elements.

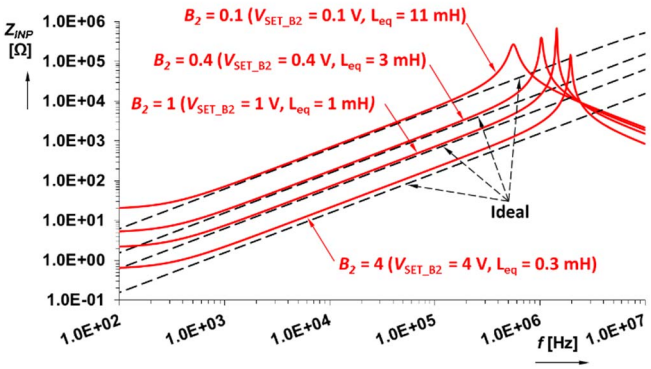

Fig. 6. Magnitude of input impedance vs frequency plot of the circuit in Fig. 4 for four different settings of DC voltage V_{SET_B2}.

As can be seen, parameter B_{B1+CA} remains at the position in numerator part of the function and parameter B_2 in the denominator part of the function. The increased number of elements in the equation represents cost for the intended features, but now the device offers additional level of electronic controllability.

Not only the lossy or lossless type of impedance (immittance) character can be set but even the equivalent inductance value (shift of the trace in magnitude characteristics) can be tuned by B_2 now (Fig. 6).

IV. Substitution Capacitance for Cosntant Phase Element

Interesting results for the input impedance in lossy mode were obtained for standard integer-order capacitor C when it was replaced by the passive version of the fractional order element, so-called CPE [20], [25] (Fig. 5). The whole procedure of the CPE design can be found in [25]. The overall impedance of the CPE30 is expressed as $Z_{CPE}(s) = 1/s^{\alpha}C_{\alpha}$, where $C_{\alpha} = 1/X_{CPE\alpha}$ and the order $\alpha = \varphi/90$.

Therefore, $\varphi = 30\ ° \rightarrow \alpha = \varphi/90 = 1/3$ and $X_{CPE\alpha} = 10$ kΩ. As clear from Fig. 7, lossless character changes into lossy character

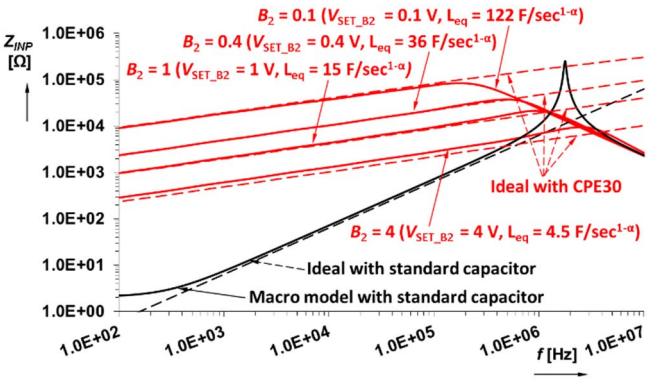

Fig. 7. Fractional-order input impedance characteristic for different settings of V_{SET_B2} (implementation of CPE30 [25]) compared with standard capacitor.

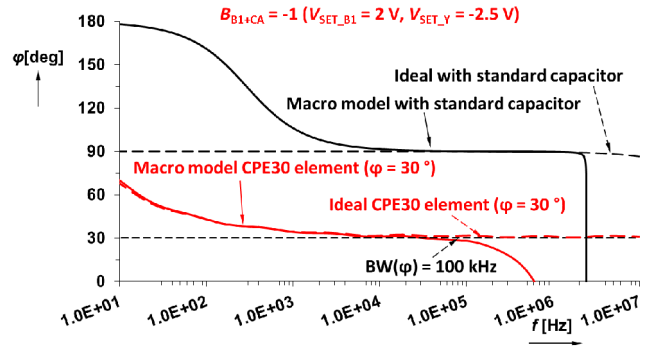

Fig. 8. Phase response characteristic of synthetic inductor with CPE30.

when the CPE is used for setting of $B_{B1+CA} = 1$ ($V_{SET\_B1} = 2$ V, $V_{SET\_Y} = -2.5$ V) and specific settings of B_2. Input impedance value starts from 550 Ω at frequency 100 Hz.

High-frequency operational range remains almost the same. The interesting results are evident in phase responses (Fig. 8). Subtracting the integer-order and fractional-order traces, the gained phase shift represents value of the CPE ($\varphi = 30$ °) itself. Operational frequency range falls between 1 kHz and 101 kHz.

V. CONCLUSION

The novelty of this paper consists of proposed structure of the synthetic element (synthetic inductor) and its tunability. This paper deals with the procedure of the designing of such a structure and describes all important parameters including the theoretical characteristics and results simulated in PSpice. The device performs valid operation in the range of frequencies from 100 Hz up to 1.5 MHz (simulated in Fig. 3 and Fig. 4) for $B_{B+CA} = 1$ (the lossless character) and $B_{B+CA} = -1$ (the lossy character). Fig. 4 shows the confirmation of the theoretical expectation and changes its phase for the lossless setup from 180 ° to 90 ° and for the lossy setup from 0 ° to 90 ° limiting at higher frequency of 2 MHz. The simulation results of the function (5), based on the circuitry in Fig. 5, are shown in Fig. 6. It indicates behavior for different setting of V_{SET_B2} (tuning of equivalent inductance). The resulting traces are given in Fig. 7 (behavior obtained for a replacement of integer-order capacitor by fractional-order CPE30 [20]) where the phase response respects the phase shift of CPE30 in bandwidth of $BW(\varphi) = 100$ kHz (a limitation of the bandwidth is allowable phase ripple of CPE30 and it is further described in [20]). The proposed structure brings interesting results in the field of synthetic elements which are expected to be useful in the development of further applications (for example in fractional-order resonators [26]-[27]).

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E Electronically Reconfigurable and Tunable Fractional-Order Filter Using Resonator Concept and Feedforward Path for Low-Frequency Tone Signalization

Objective 3; (impact factor (2022): 3.476)

Outline

Bibliographic Information

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Author's Contribution

Extensive investigation and preparation of the state of the art based on proposed methodology and related works (based on general comparison of the transfer response, electronically reconfigurability, power consumption, frequency usability, etc.). Processing measurements and visualization of results of the manuscript. The author wrote a significant part of the manuscript while also working on the finalization of the manuscript, i.e. multiple reviews, copy-editing, etc. The proposed solution introduces

distinctive transfer responses, not present in conventional models, that have significant potential in various applications, such as adaptive frequency equalizers and a random distortion level control. For instance, the fractional-order resonator implementation may be used in the phase/frequency detection or in achieving synchronization between two signals of the same frequency and phase. This paper adds solution for Objective 3.

Author's contribution: 40 % (the main author).

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Electronically Reconfigurable and Tunable Fractional-Order Filter Using Resonator Concept and Feedforward Path for Low-Frequency Tone Signalization

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ABSTRACT A novel electronically reconfigurable fractional-order filter allowing independent electronic frequency tuning and switchless change of the transfer response by a single parameter between standard band-pass, inverting all-pass response and special type band-reject response is presented in this work. The differences between these special transfer characteristics and standard features consist in magnitude and phase response behavior. Inverting amplification or attenuation is also available. The filter has tested frequency range between 1 Hz and 100 kHz. The proposed fractional-order filter (using two fractional-order element having equivalent capacity 8.7 uF/sec^1/4, $\alpha = 3/4$) tunability yields one-decade range approximately between 10 Hz and 100 Hz by transconductance between 0.19 and 1.1 mS (fractional-order design helps with reduction of driving force less than one decade). The application example in frequency/phase detector (operationability around center frequency 100 Hz - between 50 and 180 Hz) and further signaling frequency detecting system for frequency shift keying demodulator offers maximal detectable voltage (about 300 mV) for alignment (zero phase shift) of the signals of the same frequency (center frequency of the proposed filter in inverting all-pass mode). It also offers an interesting application in frequency shift keying demodulation process (or for identification/signalization purposes of certain frequencies) by usage of a simple additional comparator generating clear output state. Cadence simulations as well as experimental tests using integrated cells of special multipliers fabricated in ON Semiconductor 0.35 μm I3T25 CMOS process confirm operationability of the proposed concept as well as simple application of special response of the filter for phase/frequency detection and demodulation purposes.

INDEX TERMS Active filter, electronic adjustment, fractional order, operational transconductance amplifier, resonator, switchless adjustment, transfer response reconfiguration.

I. INTRODUCTION

In many cases, signal processing and readout systems require modification of transfer response (the type of transfer response, bandwidth limit, etc.). In such cases, only tunability or multifunctionality (manual selection of the output type of response by switches) is insufficient [1], [2]. Reconfiguration of the transfer response of a filter cannot be solved by standard active devices (operational amplifiers) because many degrees of freedom are expected (pass-band gain, pole frequency, etc.) [3].

Fractional-order (FO) circuits [4] bring new features to this field because areas between stop-bands and pass-bands can be set with less steepness than in integer-order cases. It is consequence of the magnitude slope dependence on frequency and its direct relation with the order of the FO devices used in the design [5]. Complex structures of many integrators in feedback loops [1], [2] offer reconfiguration of the slope of response by selection of an appropriate output of the integrator [5]. The full reconfiguration of transfer response (switchless change of transfer response) requires

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more extensive modifications, degrees of freedom and coordination (suitable setting and simultaneous adjustment) of driving forces – DC voltages [6]. Specific requirements on the slope of response can be fulfilled by FO approaches [4]. These requirements depend on specific applications.

The following part of the work introduces corresponding topics and highlights advantages of the presented solution among already studied and analyzed concepts in the field of reconfigurable filters. Specific setting of the filter has an interesting and unusual application for frequency/phase detection. It is important to note that presented combinations of magnitude and phase responses are also unavailable in standard integer-order concepts (without reconfigurable features).

A. RECONFIGURABLE FILTERS

Reconfigurable filters [3] can be used with high benefits for equalization (modification and optimization of gains in various frequency bands based on current conditions of transmission environment or requirements of a system) of a communication channel. The most important feature of these types of filters consists in a single-input single-output topology.

The transfer response is not selected at several input or output terminals but established by appropriate setting of the parameters of topology (in many cases continuously). Several topologies in standard circuit theory (lumped elements) have been reported in [3] but significant attention is especially devoted to higher radiofrequency (RF) bands (GHz) due to the easiest construction of these devices (electromagnetically coupled elements). In these RF bands, the switchless change of transfer response can be easily solved even in passive solutions [7]–[11]. Research in this field especially targets on microwave systems. However, in the field of low-frequency applications, it is not an easy task. Special active elements having various degree of freedom (multiparameter adjustability) and extensive complexity of active circuitry are required [5]. Microwave-based concepts use electromagnetic couplings existing in RF bands (higher than MHz), which is not easily available for low-frequency signals. These concepts have certain advantages of power consumption because majority of these circuits, except biasing of diodes for tuning [10], [11], does not require power supply [7]–[9]. However, very high geometrical accuracy of the designs must be ensured. In some cases, reconfiguration is given by micro-electro-mechanical systems (MEMS) based switches [9]. If there are electronic adjustable features (i.e. center frequency or bandwidth adjustment), they are concentrated to PIN diodes, varactors [10], [11] or even mechanical switches [9] that are not allowing continuous adjustment. In order to see conceptual differences, typical solutions using lumped elements as well as microwave approaches are compared in Table 1. The analysis of solutions, presented in Table 1, leads to the following conclusions:

a) resonators are not frequently used for design of reconfigurable filters in standard lumped elements-based approaches (it is a significant domain of microwave circuits) [3]–[6];
b) the highest degree of reconfigurability of the filter requires a complex circuitry and multiparameter adjustable active elements [5], [6];
c) the adjustment of the order reconfiguration influences the slope between pass and stop band, without change of the transfer type [5];
d) the number of available transfer responses in microwave resonator based approaches is either quite low [7], [8], 10] or does not include band-pass (BP) response (it is the most frequently used response in many applications) [7], [8];
e) the adjustment of microwave filters has not electronic character [7]–[9], only several cases include some electronic adjustment employing variable capacity of diode (varicap) by bias voltage [10], [11];
f) transfer responses of special character (untypical behavior of magnitude and phase responses) together with simple amplification simultaneously) are not available and studied.

Important advantage of our concept consists in utilization of basic active devices without mutliparameter feature (allowing extended degree of freedom) but sufficient for expected purpose of electronic tunability and transfer reconfiguration. Based on Table 1, no design was target to low-frequency domain. Standard ideal integer-order LC resonator cannot be used in the presented solution because of instability when certain conditions are fulfilled. Therefore, some settings of the presented circuit, using integer-order elements, will cause instable operation (BP response especially). On the other hand, the utilization of FO elements makes the solution stable. The main results of the analysis of solutions indicated by Table 2 show the following:

a) there is no relation between reconfiguration of transfer responses and variation of parameters of FO device when a passive FO device is used [6], [15], [16];
b) electronic tuning (center, pole frequency) does not require modification of the set of parameters when a passive FO device is used [6], [15];
c) the passive FO device must be completely replaced when the change of order is required [6], [15], [16];
d) electronic tuning requires modification of the set of parameters when active solution of FO filter (the FO character is approximated by higher-order filter response [13]) is used [13], [14];
e) active solution of FO character offers electronic setting of the order [12]–[14], [17] but topology is very complex (many active elements [13], [14]) requiring many degrees of freedom of many parameters [13], [14];
f) electronic adjustment of stop-band attenuation (in order to set useful as well as undesirable spectral components properly) of the BP response is not solved in the reported cases;
g) previous solutions do not use resonator concept;

h) in some works [12], [14], [17], the number of transfer responses is quite low;
i) the input impedances are not high and output impedances are not low simultaneously in several promising structures (for immediate application in voltage mode) [6], [13]–[15]. However, it cannot be considered as a direct disadvantage in current-mode solutions [5].

Very often, solutions approximating FO Laplace operator have a complex topology [13], [14], [18], [19]. However, it is a cost for beneficial reconfigurable features (tuning and transfer response reconfiguration) of the filter (electronically). Reconfiguration of the order and transfer function is also available in works [18], [19] but solved by switches and decoders discontinuously. Therefore, these solutions are excluded from Table 2 where continuously electronically adjustable solutions are compared.

The most important drawback of recently reported multifunction solutions consists in necessity of new set of values of parameters (matching for simultaneous change) for each change (readjustment) of the order. Therefore, utilization of the resonator concept in FO designs brings significant advantage. The FO device has fixed features – passive RC approximation) and responsibility for tuning concentrates to active elements except operational amplifiers (they offer complex and non-tunable solution of resonator [20]). The operational transconductance amplifiers (OTAs) [21] are used in our case. Moreover, the adjustment of the order can be separated from tuning when the FO device is replaced by active solution [13]. A simple core of the useful reconfigurable filtering topology, allowing special transfer functions, can be created by a simple resonator structure. There were reported several examples of fractional-order LC resonators (see Table 3) but they have some disadvantages (e.g. linear electronic tuning is not allowed [22]–[25] and high complexity [26], [27) reported in detailed comparison in [22]–[27]. Their basic principle utilizes standard Antoniou gyrators [20] with operational amplifiers for not easily tunable passive solutions and electronically adjustable OTA-based gyrator [21]. Different circuit solutions of the gyrator were obtained by current conveyors and optocouplers for electronic adjustment [27]. Our modification in the topology of [21], used in this work, brings new linear voltage control of transconductance (OTAs are created by linear multipliers) where the value of transconductance has no lower limit (can be even zero). Topology in [26] offers electronically readjustable order of the FO resonator (equivalent inductance, capacity or both). However, this useful feature results in complexity of the concept.

B. PHASE DETECTOR

Standard concepts of phase detector in frequency demodulators employ integer-order band-pass filters using basic passive elements (LC) having non-tunable properties. The phase detector solves especially phase relation between the input and reference waveforms. On the other hand, the values of amplitude have also significant influence because they determine the value of DC (or low-frequency) voltage given by the value of phase shift. In the case of standard integer-order RC and LC filters in the phase shifting path, the magnitude changes with ± 20 dB/dec around the center frequency of the filter. It may have significant impact on the DC output level and accuracy of phase shift evaluation, especially for large values of phase shift changes where magnitude response varies significantly. The presented technique offers a simple solution for the issue with magnitude increase/decrease in the input path of frequency demodulator providing phase shift for input waveform with varying frequency. Our application example shows utilization of one selected and set transfer response (inverting AP response) in phase/frequency detecting circuit. Phase and frequency detectors may find applications in many areas including communication systems [28]–[32] and low-frequency biomedical technologies [33]. Electroencephalogram (EEG) and electrocardiogram (ECG) signal readouts appreciate operation of these applications in units-hundreds of Hz [33]. Comparison of typical concepts in Table 4 shows usefulness of solutions from both topological (complexity) and performance aspects. The filters used in works [28]–[32] do not have flat magnitude responses ensuring constant amplitude for both incoming signals for multiplication. In addition, also overall complexity of detectors is larger in many works [29]–[32] than in our case. Electronic tuning of the filter brings useful feature because the operation (carrier) frequency can be easily changed (impossible in [29]) and not documented in the rest of works [28], [30]–[32]). The last work [34], regarding to this topic, has very similar features. However, there are significant differences. In this paper, the multiplier has a single output (the type of multiplier in this work and in [34] is different and has different internal CMOS topology, i.e. the doubled output voltage is not available here (not necessary here – sufficient dynamical ranges of active devices) but the topology is simpler than in [34]). Next, there is difference in the phase response of the ''filtering'' block in the frequency/phase detector. Work [34] uses a standard first-order all-pass response ($0° \rightarrow 180°$) whereas solution in our actual work employs a special response of fractional-order reconfigurable filter generating inverting all-pass response having phase limits in $\pm 180°$ ($+180° \rightarrow -180°$) with $0°$ at the target value of the detected frequency (the same as compared). It results in the maximal detected output voltage of the multiplier when the phase difference of signals of the same frequency is zero (or the input frequency of complete phase detector is identical with the setting of the filter). On the other hand, the behavior of phase detector in [34] is different. The maximal output DC voltage is available for the largest phase/frequency difference, zero voltage for alignment of the input and reference waves. The overall complexity of both circuits is similar and in [34] the power consumption is lower than in our presented solution (given by the used technology and supply voltage).

TABLE 1. General comparison of principles of filters having a feature of transfer response reconfiguration.

Reference	Solution of the filter based on resonator	Purpose	Principle	Transfer response switchless reconfiguration in the same topology without change of the FO device character	Integer order of the filter (when applicable)	Fractional-order tested (value of the order of used FO device)	Electronic adjustment (driving force)	Number of transfer response available	Type of transfers	Symmetrical magnitude slope of band pass response	Special phase responses available	Complexity (number of active / passive devices)	Complex active device (multiparameter adjustability) not required	Only grounded capacitors (or FO elements) required	Useful feature among standard tuning	Supply and power consumption	Experimentally tested (with fabricated IC)
[3]	No	Middle frequency	Multi-feedback loops	Yes	2	No	Yes	6	AP, BR, HP, iBP, HPZ, LPZ	Yes	No	4 / 2	Yes	Yes	Transfer reconfiguration	±5 V, (N/A)	Yes (No)
[5]	No	Middle frequency	Multiple leap-frog feedback	Yes	4	Yes (0.3→0.7)	Yes	1	LP of 1.-4. order	-	No	> 5 / 4	Yes	Yes	Order reconfiguration	±1,65 V, (N/A)	Yes (Yes)
[6]	No	Middle frequency	Multi-feedback loops	Yes	2	Yes (0.3→0.7)	Yes (current)	4	LP, HP, BP, BR	No	N/A	5 / 4	No	No	Transfer reconfiguration	±1,65 V, (N/A)	No (No)
[7]	Yes	High frequency	RF coupled resonators	N/A	2	N/A	No (resonator geometry-mechanical)	2	AP, BR	-	N/A	*	**	N/A	Transfer reconfiguration	**	Yes (N/A)
[8]	Yes	High frequency	RF coupled resonators	N/A	N/A	N/A	No (resonator geometry-mechanical)	2	AP, BR	-	N/A	N/A	**	N/A	Transfer reconfiguration	**	No (N/A)
[9]	Yes	High frequency	RF coupled resonators	N/A	3	N/A	***	3	BP, AP, BR	Yes	N/A	N/A	**	N/A	Transfer reconfiguration	**	Yes (N/A)
[10]	Yes	High frequency	RF coupled resonators	N/A	N/A	N/A	Yes (voltage)	2	BP, BR	Yes	N/A	- / >10	**	N/A	Transfer reconfiguration	**	Yes (N/A)
[11]	Yes	High frequency	Phase shifter + band-pass filter	Yes	1	N/A	Yes (coupled transmission lines)	3	BP, BR, DT	Yes	N/A	N/A	**	N/A	Transfer reconfiguration	**	Yes (N/A)
Proposed																	
Fig. 1	Yes	Low frequency	LC resonator + summation with adjusted input signal	Yes	2	Yes (0.75)	Yes (voltage)	4	BP, iAP, sBR, iDT	Yes	Yes	5 / 3	Yes	Yes	Transfer reconfiguration	±1,65 V, (40 mW)	Yes (Yes)

N/A – not available; s – special (nonstandard); middle frequencies: kHz – MHz; low-frequencies: Hz – kHz; high-frequency: MHz – GHz;
*planar substrate layers; ** passive; *** resonator geometry – mechanical + micro-electro-mechanical-system (MEMS);
AP – all-pass, BR – band reject, BP – band-pass, HP – high-pass, LP – low-pass, DT – direct transfer response (i – inverting, Z – with transfer zero)

C. CONTRIBUTION OF THIS WORK

Based on the above discussions, the main contribution of this work is in the design of a novel type of reconfigurable filter using specific electronically adjustable feedforward path and electronically adjustable resonator. Among others, the new feature of the filter consists in simultaneous availability of BP (order of passive FO elements allowing the set of magnitude slope of attenuation), inverting all-pass (iAP), and special band-reject (sBR) response having a common magnitude response and special phase response not available in standard range between $0 \rightarrow \pm 90°$ (integer order case – 2^{nd} order circuit) but in range of $+180° \rightarrow -180°$. The proposed filter offers features (available simultaneously) which are not standardly available and discussed in similar solutions:

a) several types of magnitude and phase responses available by electronic reconfiguration (single parameter);
b) stable operation of LC resonator without dumping (impossible in ideal integer-order systems – issues with stability);
c) a resonator-based concept excluding utilization of floating passive elements;
d) a concept useful for specific demand on the slope of attenuation (fitting for FO circuit applications – cannot be solved by integer-order circuits);
e) high input and low output impedances and
f) electronically adjustable active devices (OTAs) that allows to set both polarities of transconductance (useful in reconfigurable systems) for complete electronic control (tuning, switchless transfer response configuration) of the proposed filter. Note that the presented method of transfer response reconfiguration does not suppose any change (modification) of the FO device (independent on the order and inductive or capacitive character).

The application example in phase/frequency detection (for demodulation or synchronization purposes) indicates a simple circuitry and easily electronically tunable input/carrier frequency. Therefore, features of the system can be easily modified.

D. ORGANIZATION

This paper is organized as follows. Introductory section shows comparison of the proposed solution and its application with hitherto published works and explains motivation and contribution of this work. Section II introduces the proposed concept and its principle. Section III describes the used active elements. Experimental verification of the proposed filter and its application is presented in Section IV. Section V concludes this work.

II. PROPOSED SOLUTION OF SPECIAL FRACTIONAL-ORDER FILTER

The FO filter, shown in Fig. 1, offers reconfigurable features that are useful for further applications. The proposed topology includes two feed-forward branches performing adjustable inverting amplification and tunable FO band-pass filter based on an LC resonator. The sum of both branches creates the target reconfiguration. This technique is similar to the so-called Shadow filter operation [35] (difference is in the orientation of loop transfer) and it represents certain alternative targeting on the reconfiguration of transfer

TABLE 2. Specified comparison of lumped elements based recent switchless transfer response electronically reconfigurable (continuously) fractional-order active filters.

Reference	Year of publication	Continuous electronic tuning of filter (center frequency) documented	Matching of set of parameters not required for frequency tuning	Electronic continuous switchless reconfiguration of response (driving force) in the identical topology	Number of available transfer responses	Type of transfers	Symmetrical (magnitude slope) BP presented	Topology based on resonator	Special magnitude and phase responses available	Single parameter continuous electronic adjustment of stop-band attenuation of BP response possible	Solution of FO device (or approximant of Laplacian operator)	Transfer response reconfiguration without change of the FO device properties	New set of parameters not required for order change	Electronic setting (continuous) of the order	Number of active / passive devices	Grounded capacitors (or FO elements) required	High input impedance, low output impedance	Supply and power consumption	Experimentally tested (with fabricated IC devices)
[6]	2019	Yes	Yes	Yes	4	LP, HP, BP, BR	No	No	No	N/A	Passive (RC approximant)	Yes	Yes	No	5 / 4	Yes	No, No	±1.65 V, (N/A)	No (No)
[12]	2010	Yes	N/A	N/A	2	LP, HP	N/A	No	No	N/A	Active	N/A	No	Yes	*	-	Yes, Yes	N/A, (N/A)	Yes (No)
[13]	2017	Yes	No	Yes	4	LP, HP, BP, BR	Yes	No	No	No	Active	N/A	No	Yes	7/11 / 2/4	Yes	Yes, No	1.5 V, (N/A)	No (No)
[14]	2017	Yes	No	Yes	2	HP, LP	N/A	No	No	N/A	Active	N/A	No	Yes	7 / 3	Yes	No, No	N/A, (N/A)	Yes (No)
[15]	2019	Yes	Yes	Yes	4	LP, HP, BP, BR	No	No	No	Yes	Passive (RC approximant)	Yes	Yes	No	6 / 2	No	No, No	N/A, (N/A)	Yes (Yes)
[16]	2017	No	-	Yes	3	iDT, iHP, AP	N/A	No	No	N/A	Passive (RC approximant)	Yes	Yes	No	2 / 2	Yes	Yes, Yes	±5 V, (N/A)	No (No)
[17]	2020	No	N/A	Yes	2	LP, HP	No	No	No	N/A	Active	N/A	No	Yes	*	-	Yes, Yes	5 V, (1 W)	Yes (No)
Proposed																			
Fig. 1	2021	Yes	Yes	Yes	4	BP, iAP, sBR, iDT	Yes	Yes	Yes	Yes	Passive (RC approximant)	Yes	Yes	No	5 / 3	Yes	Yes, Yes	±1.65 V, (40 mW)	Yes (Yes)

Active solution of FO device = approximation by filter or bilinear segments; * solved as programmable analog array;
N/A – not available; s – special (nonstandard); AP – all-pass, BR – band reject, BP – band-pass, HP – high-pass, LP – low-pass, DT – direct transfer response (i – inverting, Z – with transfer zero)

responses more than on quality factor adjustment in Shadow filter design [35]. However, to the best of authors' knowledge, this approach was not presented with advantages that are discussed in this paper.

The circuit topology uses OTAs [21], [36], [37] and voltage differencing differential buffer (VDDB) [36], [37] for summing operation. The LC resonator employs an OTA-based gyrator (immittance converter and inverter [21]) where passive RC approximants of the FO passive device (constant phase element) [38]–[40] are employed (see Fig. 2). Such an implementation offers simple electronic tunability of the pole (center) frequency of the filter. Note that several attempts with sum of simple fractional and integer-order responses (integrators, differentiators) and resulting features were already studied [41], [42]. However, this work is different from previous studies due to the presence of full resonator allowing adjustable features in the topology together with adjustable feed-forward path. Considering the gain of the amplifier $A = g_{m4} \cdot R$ (and equal order α of both FO elements in topology), the complete circuitry of reconfigurable filter in Fig. 1 has the following transfer function:

$$K_f(s) = \frac{s^{2\alpha} L_\alpha C_\alpha A + s^\alpha L_\alpha \cdot g_{m1} + A}{s^{2\alpha} L_\alpha C_\alpha + 1} = \frac{s^{2\alpha} L_\alpha C_\alpha g_{m4} R + s^\alpha L_\alpha \cdot g_{m1} + g_{m4} R}{s^{2\alpha} L_\alpha C_\alpha + 1}, \quad (1)$$

where simple electronic adjustability and tunability of resonant frequency can be obtained by replacement of L_α (see Fig. 2) by synthetic equivalent [21]:

$$Z_{L\alpha} = s^\alpha L_\alpha = s^\alpha C_\alpha \frac{1}{g_{m2} g_{m3}} \cong s^\alpha C_\alpha \frac{1}{\left(k \cdot V_{SET\_gm2,3}\right)^2}, \quad (2)$$

where parameter k represents transconductance constant of the used multiplier/OTA. Then, (1) can be modified to:

$$K_f(s) = \frac{s^{2\alpha} C_\alpha^2 g_{m4} R + s^\alpha C_\alpha g_{m1} + g_{m2} g_{m3} g_{m4} R}{s^{2\alpha} C_\alpha^2 + g_{m2} g_{m3}}. \quad (3)$$

The first available transfer – BP response is obtained for $A = g_{m4} \cdot R = 0$ (i.e. $g_{m4} = 0$):

$$K_{BP}(s) = \frac{s^\alpha L_\alpha \cdot g_{m1}}{s^{2\alpha} L_\alpha C_\alpha + 1} = \frac{s^\alpha C_\alpha g_{m1}}{s^{2\alpha} C_\alpha^2 + g_{m2} g_{m3}}. \quad (4)$$

The magnitude response has slopes defined by order of CPE ($\alpha \cdot 20$ dB/dec and phase response crosses 0 ° and reaches limits $\pm\alpha \cdot 90°$ as visible in Fig. 3 for $A = 0$).

Transfer response changes to sBR filter character when $A = -1$ ($g_{m4} = 1/R$) having standard BR magnitude response but phase response having different shape than expected for standard BR (see Fig. 3):

$$K_{sBR/iAP}(s) = -\left(\frac{s^{2\alpha} L_\alpha C_\alpha - s^\alpha L_\alpha \cdot g_{m1} + 1}{s^{2\alpha} L_\alpha C_\alpha + 1}\right) = -\left(\frac{s^{2\alpha} C_\alpha^2 - s^\alpha C_\alpha g_{m1} + g_{m2} g_{m3}}{s^{2\alpha} C_\alpha^2 + g_{m2} g_{m3}}\right). \quad (5)$$

Symbolical representation (5) fits for iAP filter, but magnitude response has a character of BR filter. The phase responses of sBR has untypical behavior and phase range (see Fig. 3 and Section IV). The behavior for the value of A between 0 and -1 has very important consequences. The required value of A (negative) can be obtained by the multiplicative feature of the used specific OTA solutions or by proper polarity of transfer function (polarity of terminal selected for input of the OTA). The transfer response of inverting/noninverting follower or amplifier (abbreviated as inverting direct / direct transfers - iDT/DT) can be obtained for $A < 0$ ($A > 0$ respectively) and $g_{m1} = 0$ mS (available by multipliers).

Detailed study of (1) and variation of A between 0 and -1 by analytical form is not providing an easy survey. Therefore, a graphical solution of the ideal magnitude equation of (1) was prepared for specific condition of center frequency, which is derived below. This evaluation supposes the following definitions. The low-frequency and high-frequency band is determined by A when $s = j\omega \to 0$ or ∞, which is clearly

TABLE 3. Comparison of fractional-order resonators.

Reference	Electronic tuning	Linear dependence on driving force	Matching of parameters for electronic tuning not required	Voltage adjustment	Number of active / passive elements	Solution of FO elements	Electronic change of the order by set of parameters	Solved with fabricated IC devices
[22]	No	*	*	No	2 / 5	Passive	No	No
[23]	No	*	*	No	2 / 5	Passive	No	No
[24]	No	*	*	No	2 / 5	Passive	No	No
[25]	No	*	*	No	2 / 5	Passive	No	No
[26]	Yes	Yes	No	No	8 / 2	Active	Yes	Yes
[27]	Yes	Yes	Yes	Yes	4 / 5	Passive	No	No
Fig. 5	Yes	Yes	Yes	Yes	2 / 2	Passive	No	Yes

* standard Antoniou gyrator using operational amplifiers [20]

TABLE 4. Comparison of typical frequency/phase detectors.

Reference	Year of publication	CMOS process	Supply [V]	Power consumption [mW]	Purpose of concept	Oscillator not required in phase detection circuit	Type of used filter in structure	Ideal magnitude response of the filter is flat for all frequencies	Constant amplitude of both signals for multiplication	Detector tunable electronically for different operational (carrier) frequency	Overall complexity of phase detector (number of parts)	Overall complexity of detector (number of blocks)	Tested a processed signal levels in structures	Input dynamical range of used multipliers (OTAs) or any used element reported [mV]	Dependence of detected output voltage on phase difference shown	Maximum output voltage for zero phase difference	Experimental tests
[28]	2020	N/A	N/A	N/A	Radio-freq. systems (GHz)	No	low-pass	No	No	N/A	2	N/A	units of V	N/A	No	N/A	No
[29]	2014	0.13 µm	3.3	0.82	Middle frequency (tens of MHz)	No	RLC band-pass	No	No	No	2	3	units of V	N/A	No	No	No
[30]	2011	0.13 µm	1.2	0.26	Radio-freq. data reciever (GHz)	No	low-pass	No	N/A	N/A	2*	3	low hundreds of mV	N/A	No	N/A	Yes
[31]	2021	0.045 µm	2	485	Radio-freq. systems (GHz)	No	low-pass	No	N/A	N/A	2*	4	hundreds of mV	N/A	No	N/A	No
[32]	2017	0.13 µm TSMC	1.8	29	Radio-freq. systems (GHz)	N/A	low-pass	No	N/A	N/A	11	4	N/A	N/A	No	N/A	No
[34]	2021	0.18 µm TSMC	±0.9	5.7	Low-frequency (tens of kHz)	Yes	non-inverting all-pass	Yes	Yes	Yes	2	2	hundreds of mV	±200	Yes	No	Yes
Fig. 5	2021	0.35 µm ON	±1.65	47	Low-frequency (tens of kHz)	Yes	inverting all-pass	Yes	Yes	Yes	2	2	hundreds of mV	±500	Yes	Yes	Yes

* phase detector + LP (loop) filter for low frequency or DC output in case of phase locked loop application

visible from (1). The center frequency transfer is given as a modification of (1) where frequency dependent terms are substituted by center frequency:

$$\omega_p = \left(\frac{1}{C_\alpha L_\alpha}\right)^{\frac{1}{2\alpha}} = \left(\frac{g_{m2}g_{m3}}{C_\alpha^2}\right)^{\frac{1}{2\alpha}}\Bigg|_{g_{m2}=g_{m3}=g_{m23}} = \left(\frac{g_{m23}}{C_\alpha}\right)^{\frac{1}{\alpha}}, \tag{6}$$

to the form:

$$K_f(\omega=\omega_p) = \frac{j^{2\alpha}A + j^\alpha\sqrt{\frac{L_\alpha}{C_\alpha}}g_{m1} + A}{j^{2\alpha}+1} = \frac{j^{2\alpha}A + j^\alpha\frac{g_{m1}}{\sqrt{g_{m2}g_{m3}}} + A}{j^{2\alpha}+1}. \tag{7}$$

Graphical analysis is more effective and illustrative than complex and extensive formulas. We are searching for a point where the magnitude of $|K_\mathrm{f}|$ of the limits (for $\omega \to 0$ and ∞) equals to the gain of the BP filter at center (pole) frequency. Our theoretical discussion supposes two identical FO devices: $C_\alpha = 8.7\ \mu\mathrm{F/sec}^{1/4}$ ($\alpha = 3/4$) and center frequency 100 Hz ($\omega_\mathrm{p} = 2\pi \cdot 100$, i.e. $g_{\mathrm{m}2} = g_{\mathrm{m}3} = g_{\mathrm{m}23} = 1.1$ mS). Exemplary results and solution of this case are shown in Fig. 4. The point of intersection of lines of $|K_\mathrm{f}\ (\omega \to 0\ (\infty))|$ and $|K_\mathrm{f}\ (\omega \to \omega_\mathrm{p})|$ yields $A = g_{\mathrm{m}4} \cdot R = -0.6$. Then iAP response is obtained. Results in Fig. 4 indicate magnitude levels in low-frequency (0), high-frequency (∞) and center frequency (ω_p) positions for variation of A. The specific value of A, valid together for all three cases, yields almost constant (very small ripple) overall magnitude response of the filter (it is useful for further application). The specific configuration of the circuit allows for us to obtain a sBR filter response (phase response similar to standard iAP response in integer-order circuit) in the FO system, that cannot be commonly achieve by standard design approaches. The magnitude has

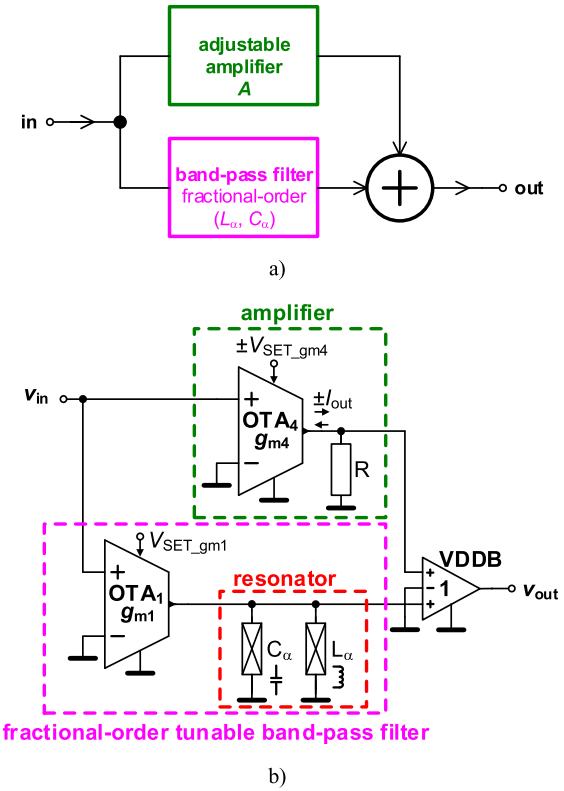

FIGURE 1. Proposed approach of reconfigurable fractional-order filter: a) block principle, b) specific scheme available by standard circuit components.

typical minimum (transfer zeros) but the phase response is not achieving the range of $0 \rightarrow \pm 90°$ but $+180° \rightarrow -180°$ (typical for iAP). From the results is clear that the center (''linear'') member of numerator of (3) or (5) respectively is not disappearing from equation as in standard integer-order case for 2nd-order BR responses. Traces (linear in interesting range) and coordinates in Fig. 3 depend on the order α, next on the values of g_{m1} and g_{m23} (L_α value) but not on the value of C_α as visible in (7). An illustrative example of ideal transfer responses for stepped A in (1) is shown in Fig. 3 (including standard ideal BR response in order to see differences from sBR). Note that the following behavior will not be available in standard integer-order circuits because standard second-order circuits (LC resonator, etc.) have unstable operation (without dumping lossy resistor as a part of LC resonator) when the linear term of denominator is missing in transfer equations (see green and black traces in Fig. 3). Integer-order example (illustrative only) in Fig. 3 is obtained for $C = 8.7$ μF and $g_{m23} = 5.47$ mS at center frequency of 100 Hz.

III. DESCRIPTION OF ACTIVE DEVICES

The presented concept employs two types of active elements fabricated in 0.35 μm I3T25 ON Semiconductor 3.3 V (± 1.65 V in our case) CMOS process. Principles of both devices with basic ideal definition of operation are shown Fig. 5. Figure 5 a) shows OTA formed by multiplier with two differential inputs and single current output. The transconductance constant has typical value $k = 1.8$ mA/V^2

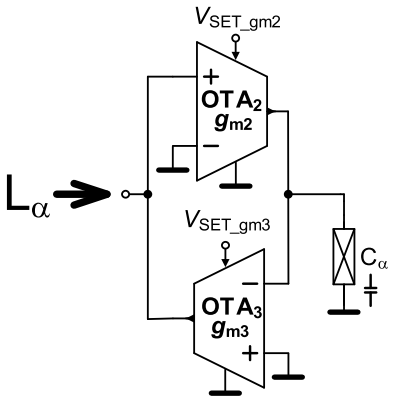

FIGURE 2. Adjustable immittance inverter and converter based on OTAs.

in Cadence Spectre simulations and 1.3 mA/V^2 in real experiments (expectable range of fabrication dispersion). The range of experimentally tested transconductance reaches $0 \rightarrow \pm 1.2$ mS (the multiplier-based concept allows to achieve a value of 0) for $V_{SET\_gm} = 0 \rightarrow \pm 0.7$ V. The bandwidth of g_m reaches more than 30 MHz for all conditions of tests [43], [44]. The dynamical range is supposed as linear for the input voltage higher than ± 0.5 V, where the total harmonic distortion (THD) falls between 0.1 and 1.5%. The terminal resistances of voltage inputs are higher than 100 MΩ and more than 100 kΩ for the current output. VDDB creates a simple sum and subtraction operation as it is captured in Fig. 5 b). The frequency response of unity-gain has a 3 dB drop at value higher than 45 MHz (all inputs). The input dynamical range reaches more than ± 0.7 V with THD below 1% (0.1% obtained for 500 mV$_{p-p}$). The voltage input resistances are higher than 100 MΩ and the voltage output resistance has a value lower than 0.4 Ω. More details can be found in [43] and [44]. The power consumption of the single multiplier and single VDDB reaches 7.8 mW and 9.1 mW respectively.

IV. EXPERIMENTAL VERIFICATION

The proposed filter was tested in simulations as well as in experiments by AC analysis. Furthermore, the filter has been utilized in a complex application example and tested in time domain. The application targets on simple frequency detection by a multiplier-based circuit. The RC approximant, so-called constant phase element (CPE) [38], [39], of the FO element ($C_\alpha = 8.7$ μF/sec$^{1/4}$, $\alpha = 3/4$) is plotted in Fig. 6. The bandwidth of constant phase range should reach at least 1 Hz – 100 kHz (tested experimentally) and the phase ripple in this band is maximally $\pm 2°$. The design of this device was performed by Valsa algorithm [38]–[40]. Note that traces (in figures) marked as ''ideal'' were gained from simulations with ideal active elements (modeled by controlled sources) and traces marked as ''theory'' are based on the discussed theoretical equations.

The values of parallel RC segments depend on the target value of equivalent capacity/inductance (pseudocapacity in our case) and on the order. The design has scalability of

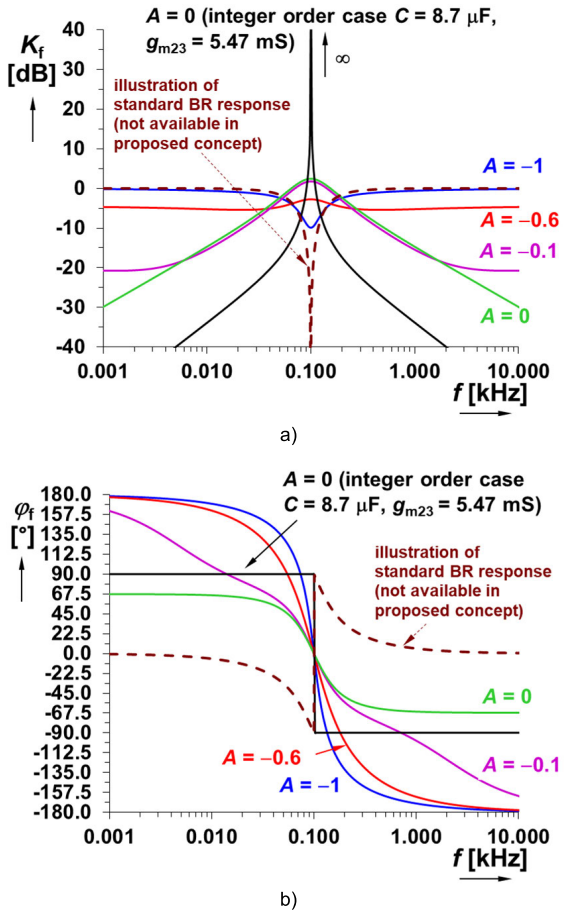

FIGURE 3. Illustration example of ideal behavior of the reconfigurable fractional-order filter: a) magnitude responses, b) phase responses.

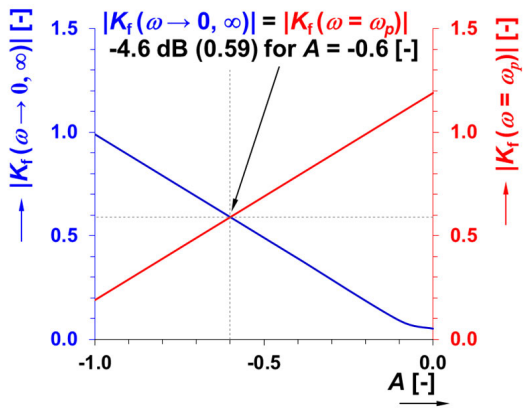

FIGURE 4. Searching for optimal value of gain A ($g_{m4} \cdot R$) giving almost flat magnitude response of the reconfigurable filter.

pseudocapacity (C_α) because not only the order but also the value of pseudocapacity is important for designers and final application. The values of the lowest "low-frequency RC segment" as well as the highest "high-frequency RC segment" have extreme values when extremely wideband (many decades, in our case theoretically from 1 Hz up to more than 5 MHz) operation and very low value of pseudocapacity (more than units of μF/sec$^{1-\alpha}$) of CPE solution are required. Our design presents a wideband CPE supposed as universal for many tests and solutions (not optimized for specific application) having quite large value of pseudocapacity (i.e. low impedance levels at lowest frequencies). It also helps in the designs using active elements having low values of terminal impedances (real parts for example around 50-100 kΩ) in order to prevent real parasitic effects in the intended bandwidths. Different magnitude impedance plots are easily available but magnitudes higher than 100 kΩ are significantly influenced by real properties of active devices (many integrated as well as commercially available operational amplifiers have terminal impedances typically in hundreds and units of MΩ). However, many frequency-selective applications (e.g. filters and oscillators) have also similar selective requirements on the validity of CPE approximation (bandwidth of constant phase zone). In many cases, tunability of standard active filters is not significantly larger than one decade (based on available ranges of adjustable parameters of active elements). Therefore, also bandwidth limitation of CPE operation may be acceptable and significantly decreases complexity of the solution (number of RC segments). On the other hand, in our case, the low-frequency design still requires "borderline" values of RC segments (large R - MΩ, large C – μF), but the high-frequency segments can be removed. Experimental tests indicate that sufficient number of segments in our application and presented bandwidth can be reduced to half of original complexity (see Fig. 6). As it was explained, the complete circuit in Fig. 6 serves also for different purposes in different bandwidths. Therefore, its design respected universal application. The exact value of passive elements was obtained by serial/parallel combinations of partial elements (SMD elements can be placed and soldered in so called sandwich form). The electronic adjustment of the order and equivalent value of CPE is possible in active form by various methods [12]–[14], [17] (the chain of bilinear sections allowing the set of zero-pole adjustments was discussed for example in [41]) after simple modification – voltage to current converter and feedback modifying two-port/filter into impedance. However, it always results in significant increase of complexity and also unsynchronized readjustability of many active parameters.

A. TESTS OF THE FILTER

The parameters of the filter were set for pole-center frequency $f_p = 100$ Hz (gain $A = g_{m4} \cdot R$ varies for obtainment of iAP, BR, sBP and iDT responses). Ideal calculation of the features (for ideal results see Fig. 3) of the filter is given in Section II ($g_{m2} = g_{m3} = g_{m23} = 1.1$ mS, $g_{m1} = 1$ mS, $R = 1$ kΩ, $g_{m4} = -1.1, -0.6, -0.1$ and 0 mS). Note that there is no specific filter approximation selected.

The AC analysis was performed for all possible configurations of the filter. The results of analysis including all necessary parameters and driving voltages are shown in Fig. 7. The frequency responses show evident dependence of stop-band gain in low- and high-frequency corners. The inverting amplifier/follower (iDT only; DT has difference in phase response only) was verified for $A = -1.1$ ($g_{m4} = 1.1$ mS) and

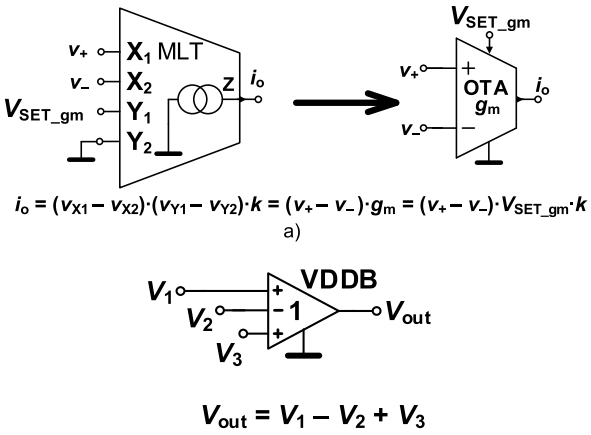

FIGURE 5. Principle of operation of active devices used for construction of the special fractional-order reconfigurable filter and its application: a) analog multiplier for application as OTA, b) voltage differencing differential buffer.

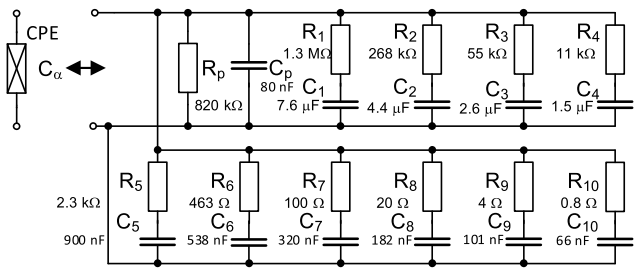

FIGURE 6. RC approximant of constant phase element used in experiments ($C_\alpha = 8.7\ \mu F/sec^{1/4}$, $\alpha = 3/4$).

$g_{m1} = 0$ mS as visible in Fig. 8. The function of amplifier can be obtained for the same setting where A will be positive. The ideal traces in Fig. 8 a) and b) were obtained by simulations with ideal controlled sources representing active elements. The DSOX-3024T oscilloscope has been used (option of frequency response analysis) for all AC analyses below (the amplitude of the input signal is equal to 100 mV). The filter has center-frequency tunable properties covered by synthetic form of L_α ($g_{m2,3}$), see (6). However, this adjustment also varies with pass-band gain. Therefore, g_{m1} must be varied simultaneously too ($g_{m1} = g_{m2} = g_{m3} = g_{m123}$). The driving of g_m (allowed in specified range $0 \rightarrow \pm 1.2$ mS ensures at least one-decade tunability (required $g_m = 0.19 \rightarrow 1.1$ mS, i.e. $V_{set\_gm123} = 0.11 \rightarrow 0.61$ V) and adjustment of gain of the feedforward path of the filter at least $0 \rightarrow \pm 1.2$ (when amplifier uses loading resistor of value 1 kΩ). Example of tuning of f_p between 10 Hz and 100 Hz (the measured values are 10.7 Hz and 105 Hz and simulation gives 11.1 Hz and 114 Hz) yields value of $g_{m123} = 0.19$ and 1.1 mS. The response of BP and iAP is captured in Fig. 9 and Fig. 10, respectively.

The value of equivalent quality factor $Q = f_p/BW$ (BW – 3 dB bandwidth) has almost constant value varying nonessentially in a range from 0.86 to 1.02 (the nominal value is 0.88) and for full tunability the range is between 11 and 114 Hz, as it is visible in Fig. 11. Consequently, the quality factor has no dependence on tunability of the filter. The gain at the center frequency can be calculated as a magnitude from (7). The power consumption of the filter reaches 40 mW (supply voltage ±1.65 V).

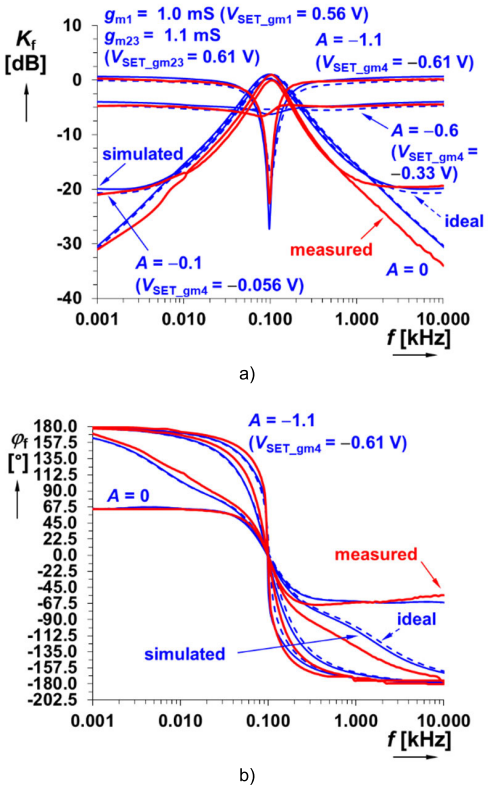

FIGURE 7. Example of important frequency responses of reconfigurable filter, shown in Fig. 1, at $f_p = 100$ Hz: a) magnitude responses, b) phase responses.

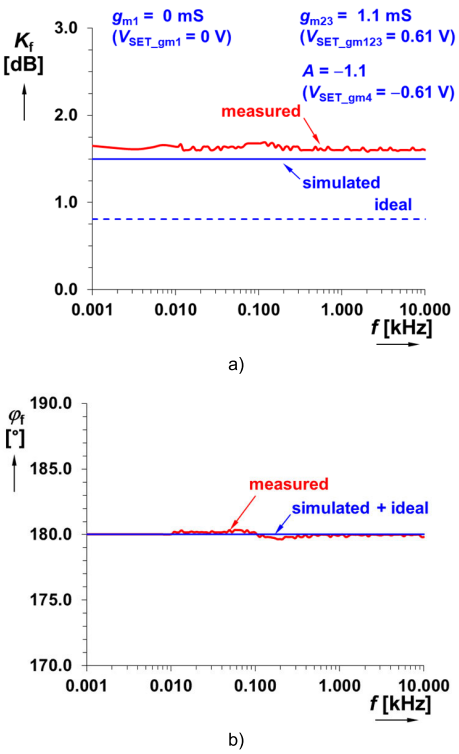

FIGURE 8. Inverting amplifier/follower responses of reconfigurable filter in Fig. 1: a) magnitude responses, b) phase responses.

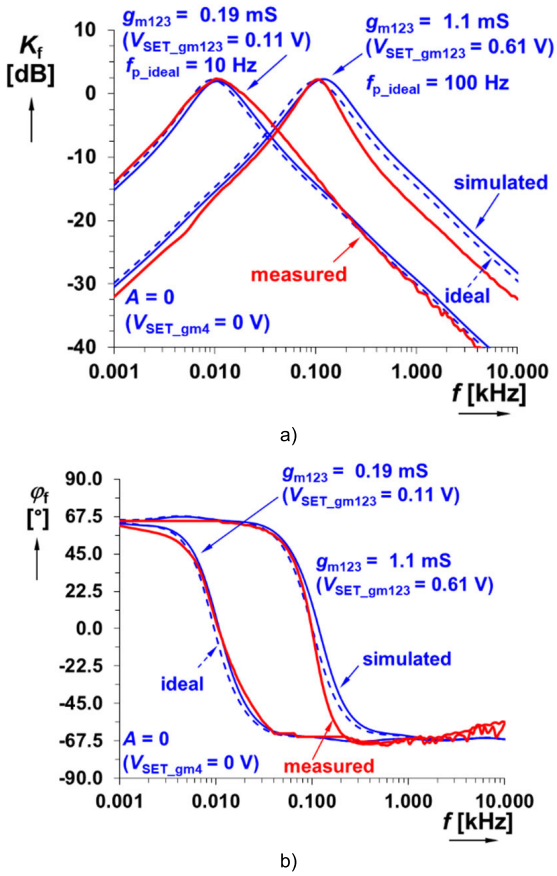

FIGURE 9. Tuning example of band-pass responses of reconfigurable filter in Fig. 1: a) magnitude responses, b) phase responses.

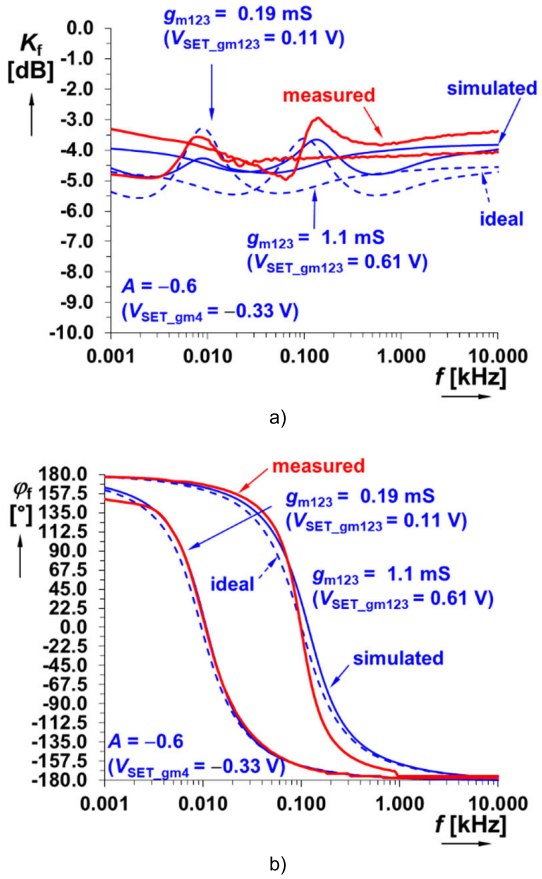

FIGURE 10. Tuning example of inverting all-pass responses of reconfigurable filter introduced in Fig. 1: a) magnitude responses, b) phase responses.

The filter was tested by Monte Carlo (MC) statistical variation as well as by Process, Voltage, Temperature (PVT) and Corner analyses. Note that the CPEs are excluded from these tests because of their discrete solution (values of capacitors on IC are not available – only active devices are included on the chip). However, these tests for CPE itself are available in [27].

Fig. 12 shows the results from MC analysis (100 runs) for BP response at nominal setting (f_p = 114 Hz, V_{set_gm123} = 0.61 V, g_{m123} = 1.1 mS in the case of simulations). Statistical results indicate deviations between minimal and maximal values of center frequency f_p from 101 up to 127 Hz (the nominal value is 114 Hz with a dispersion/standard deviation up to 4.4 Hz). The minimal and maximal Q reaches values between 0.85 and 0.91 (nominal 0.88) with a standard deviation of 9.5 m.

The effects of PVT corner analysis on the performance of BP are shown in Fig. 13. The center frequency varies between 83 and 204 Hz while the quality factor is between 0.85 and 1.02. The effects of temperature variation, tested between 10 and 40 °C, have impact on the BP magnitude response (see Fig. 14). In this case, the frequency varies between 95 and 145 Hz while the value of Q is between 0.85 and 0.93. Fortunately, all possible deviations can be easily compensated by electronically tunable features of the filter.

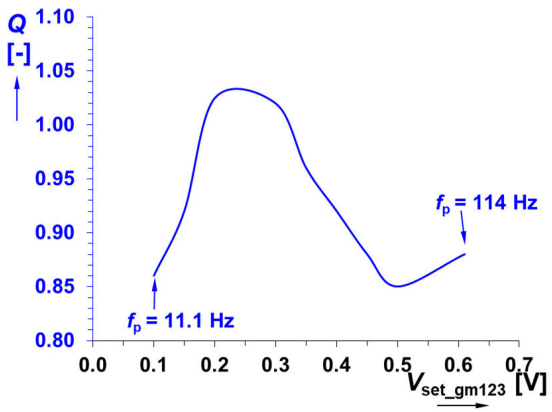

FIGURE 11. Dependence of quality factor of the BP response on driving voltage V_{set_gm123} (simulation).

We have also tested iAP response on MC deviations at the same conditions because iAP is an important part of further application (frequency/phase detector). The variation of frequency f_p, where phase equals to 0°, reaches minimal and maximal values between 97 and 123 Hz (standard deviation is around 4 Hz). The worst case gain (attenuation

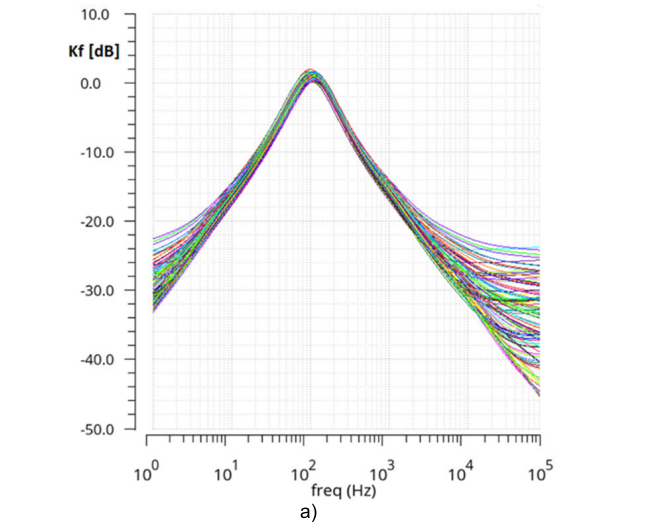

FIGURE 12. The Monte Carlo analysis results for BP response: a) 100 runs of magnitude responses, b) histogram of statistical variations of f_p, c) histogram of statistical variations of Q.

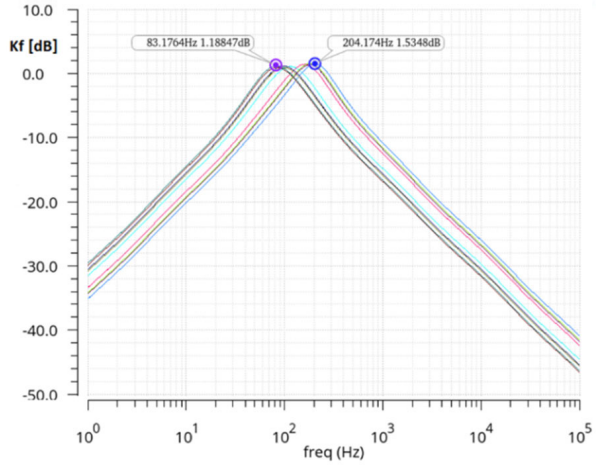

FIGURE 13. Effect of PVT corner analysis on BP magnitude response.

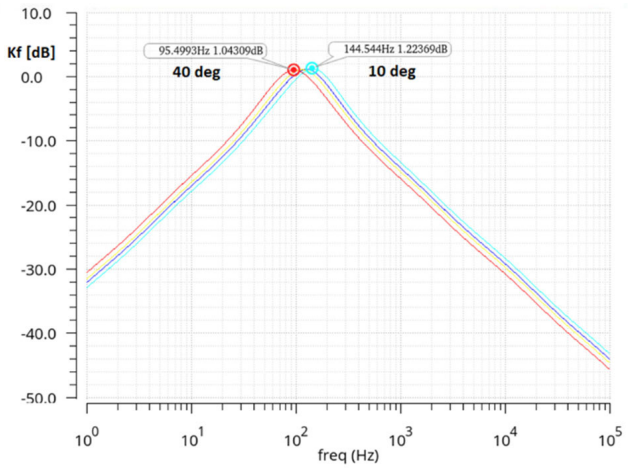

FIGURE 14. Effects of temperature analysis on BP magnitude response.

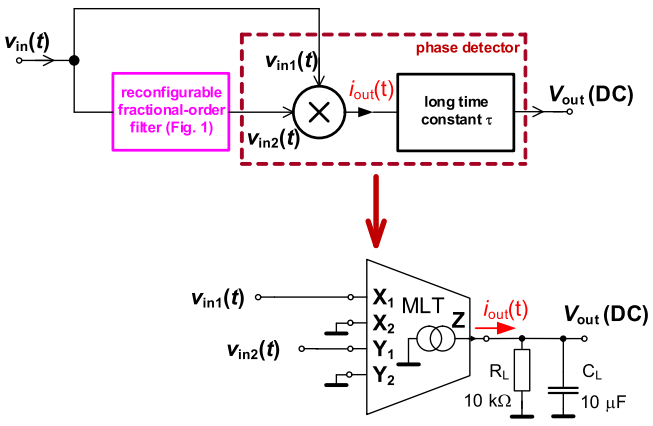

FIGURE 15. Proposed application of the frequency detector – a circuit solution.

respectively) deviation (ripple of the flat magnitude response) reaches −4.5 ±3.5 dB (typically lower value about ±1.5 dB). The PVT corner effects cause significantly worse results in accuracy than MC (±5 dB in the magnitude as the largest value in the whole bandwidth). The temperature effects itself yield maximal ±3.5 dB variation of the gain and f_p between 93 and 137 Hz. All these results are expectable and have acceptable and easily compensable values with respect the dependence of key parameters of the filter (g_m of active elements especially) on PVT corners, temperature and statistical mismatch.

B. APPLICATION EXAMPLE OF RECONFIGURABLE FILTER – PHASE/FREQUENCY DETECTOR FOR FREQUENCY DETECTING SYSTEM OF FREQUENCY KEYING DEMODULATION

Transfer of the reconfigurable filter (see Fig. 1) offers a flat magnitude response in iAP mode useful for further applications. Such a setting (see Fig. 10) ensures operation without influence of magnitude slope changes on detection procedure in comparison with BP response. This design yields pass-band attenuation of the v_{in2} voltage about 4-5 dB with maximal magnitude change (fluctuation) 1-2 dB (between 1 Hz and 10 kHz) and center frequency of BP filter $f_{\text{p}} = 100$ Hz. The system of frequency detector is shown in Fig. 15. The resulting maximal output DC voltage (or signal of very low frequency – Hz, sub-Hz) of the detector is approximately determined as follows ($V_{\text{in1,2}}$ are amplitudes):

$$V_{out\_\max}(\tau \ll t) \cong \frac{V_{in1}V_{in2}}{2} \cdot k \cdot R_L \cdot \cos(\varphi[rad]) \cong \frac{V_{in1}^2}{2} \left|K_f(\omega)\right| \cdot k \cdot R_L \cdot \cos(\varphi[rad]), \quad (8)$$

This equation is valid for time larger than time constant of the detector ($R_{\text{L}}C_{\text{L}} = \tau = 100$ ms). As it is visible from (8), a flat magnitude is required for precise frequency demodulation purposes. Otherwise, variation of $v_{\text{in2}}(t)$ (in the case of BP configuration of the filter in Fig. 15 – low- and high-frequency areas of magnitude slope outside of -3 dB band) cause significant impact on the value of $V_{\text{out\_max}}$ (DC). Supposing $|K_{\text{f}}(\omega)| \cong$ const. (due to our reconfigurable filter), the value of $V_{\text{out\_max}}$(DC) depends on the amplitude of v_{in1} and phase shift between the input signals of the multiplier. The phase shift of the iAP filter in the detector has a complex form as can be seen in (9), as shown at the bottom of the page. Equation (9) can be substituted to (8) in order to express the dependence of $V_{\text{out\_max}}$(DC) on input frequency.

The frequency dependence of the phase difference between the output and input wave of the reconfigurable filter (iAP response) is shown in Fig. 16. Validity of (9) for $V_{\text{out\_max}} > 0$ V limits into the range between 50 Hz and 180 Hz. Therefore, results are provided in this range.

Dependences of v_{in2} (output of the reconfigurable filter) and output DC voltage $V_{\text{out\_max}}$ on phase difference and frequency are shown in Fig. 17. The voltage amplitude v_{in1} is equal to 250 mV while v_{in2} (attenuated by 4-5 dB) reaches approximately 145 mV. The maximal value of the detected DC voltage $V_{\text{out\_max}}$ indicates phase equality between v_{in1} and v_{in2}, i.e. the input frequency having a value of center/pole frequency of current adjustment of the reconfigurable filter.

Once again, the ideal curves in Fig. 16 and Fig. 17 were obtained at simulations with controlled sources (ideal). The theoretical curves, on the other hand, were obtained by direct substitution of numeric values to the derived equations (8) and (9).

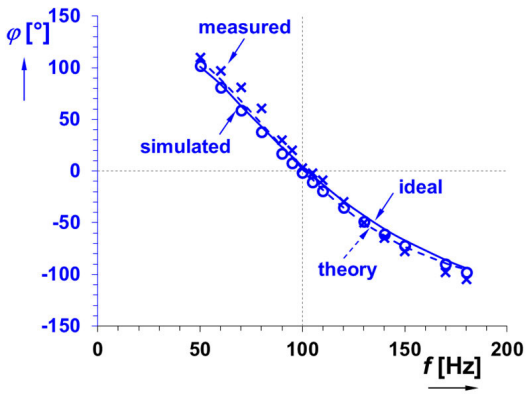

FIGURE 16. Dependence of phase difference (phase shift) of the reconfigurable filter in frequency detector on input frequency.

Typical examples of time responses of the system are captured in Fig. 18. These results also confirm that the maximal output voltage is reached for the input frequency identical with the center frequency of reconfigurable filter in the detector. In other words, it means alignment of the input and reference wave or wave produced at the output of the filter (iAP transfer is configured). When the maximal voltage is reached (≅300-320 mV) then the input frequency is equal with the center frequency (100 Hz) and phase shift between both waves is zero. Power consumption of the application reaches 47 mW at supply voltage ±1.65 V.

The final practical application example of the proposed phase/frequency detector consists in Frequency Shift Keying (FSK) demodulation [45]. The detector can be utilized for detection of specific spectral components in slow and low-frequency signals of various natural sources (EEG, ECG, etc.) [33] or in power line communication [45]. The output of the phase detector is connected to the comparator with thresholds as it is shown in Fig. 19. The comparator uses the VDDB device from Fig. 5 b). The feedback from the output to the positive input creates an amplifier with very high (in ideal case infinite) gain. The second positive feedback using resistive dividers serves for definition of two threshold levels:

$$v_{out\_ref\_HL}(DC) \cong \left(\frac{R_2}{R_1 \| R_3 + R_2}\right) V_{DD}$$
$$v_{out\_ref\_LH}(DC) \cong \left(\frac{R_2 \| R_3}{R_2 \| R_3 + R_1}\right) V_{DD}. \quad (10)$$

The resulting values of resistors for $v_{\text{out\_ref\_HL}} = 200$ mV and $v_{\text{out\_ref\_LH}} = 150$ mV are shown in Fig. 19 (hysteresis of 50 mV used for better noise immunity). The output level varies between L state (0 V) and H state (3 V). The output

$$\varphi(\omega) = \tan^{-1}\left\{\frac{L_\alpha g_{m1}\omega^\alpha \sin\left(\frac{\pi}{2}\alpha\right) - C_\alpha L_\alpha^2 g_{m1}\omega^{3\alpha}\sin\left(\frac{\pi}{2}\alpha\right)}{A + A\left(C_\alpha L_\alpha \omega^{2\alpha}\right)^2 + L_\alpha g_{m1}\omega^\alpha \cos\left(\frac{\pi}{2}\alpha\right) + AC_\alpha L_\alpha \omega^{2\alpha}\left[4\cos^2\left(\frac{\pi}{2}\alpha\right) - 2\right] + C_\alpha L_\alpha^2 g_{m1}\omega^{3\alpha}\cos\left(\frac{\pi}{2}\alpha\right)}\right\}. \quad (9)$$

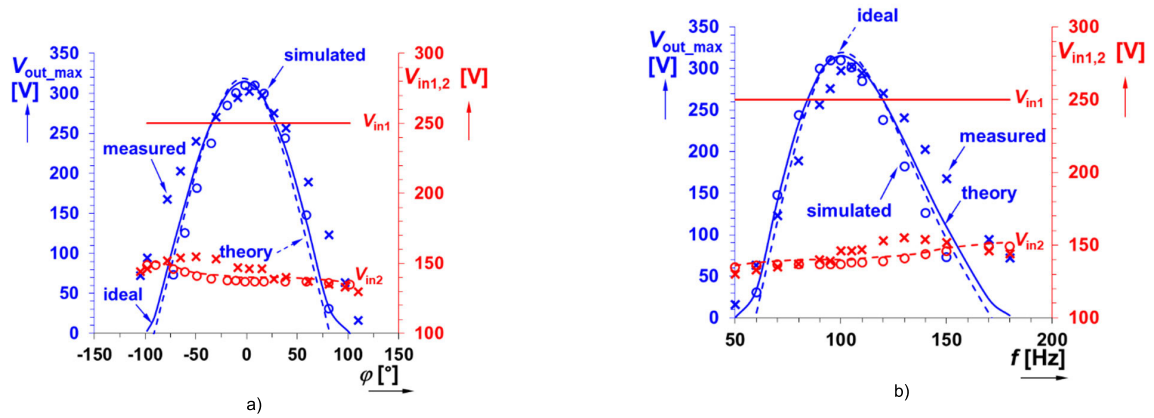

FIGURE 17. Response of the output voltage level of the reconfigurable filter and output voltage of the frequency detector on: a) phase difference, b) input frequency.

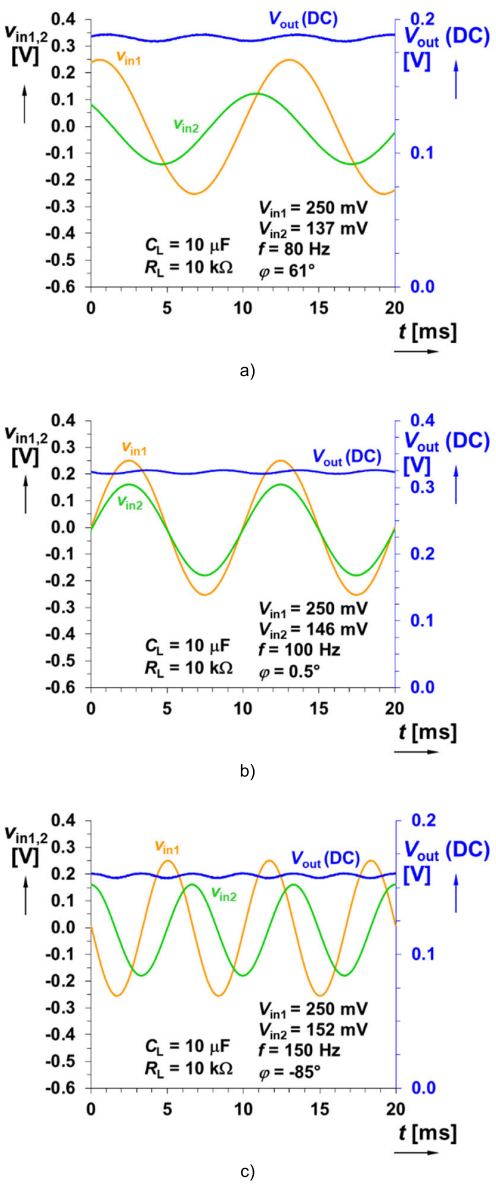

FIGURE 18. Experimental time responses of the detecting system for three different frequencies (phase shifts): a) 80 Hz, b) 100 Hz, c) 150 Hz.

drive of VDDB causes 300 mV voltage drop [43], [44]. The signaling frequency is set to 100 Hz. Based on Fig. 17 b), i.e.

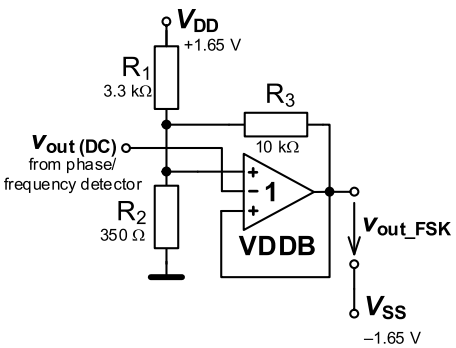

FIGURE 19. Comparator with hysteresis for signaling frequency detecting part of FSK demodulator.

knowledge of thresholds, the frequency below 80 Hz (in the experiments was set to 70 Hz) or above 130 Hz means output voltage of the frequency detector below 150 mV (below the H → L threshold level) and frequency around 100 Hz generates the maximum voltage at the output of the detector (around 300 mV) that is sufficiently above the H → L threshold level. Therefore, the presence of 70 Hz signaling frequency at the output results into state H (3 V) and frequency 100 Hz changes the output into state L (active state in this case) (0 V). It is compatible with 3.3 V logic for immediate digital processing. Please note that, in these considerations, the reference ground refers to V_{SS} (−1.65 V) at the output of the comparator. Furthermore, these features can be easily modified for specific design cases.

Employment of the frequency detector with adjustable frequency (the peak character of the response is captured in Fig. 17) is useful for decision-making systems in multi-tone modulations because frequency adjustment of the detector (f_p) and setting of comparator can be precisely adjusted (at the required value of frequency and sensitivity/selectivity) in order generate the output state (v_{out_FSK}). In other words, the change of state occurs only when the input frequency almost equals to value of the expected (set) frequency of the filter in detector. Such an example of operation is shown in Fig. 20, where the effect of additional comparator is demonstrated for evaluation of decision between two exemplary input frequencies (70 and 100 Hz) provided by the

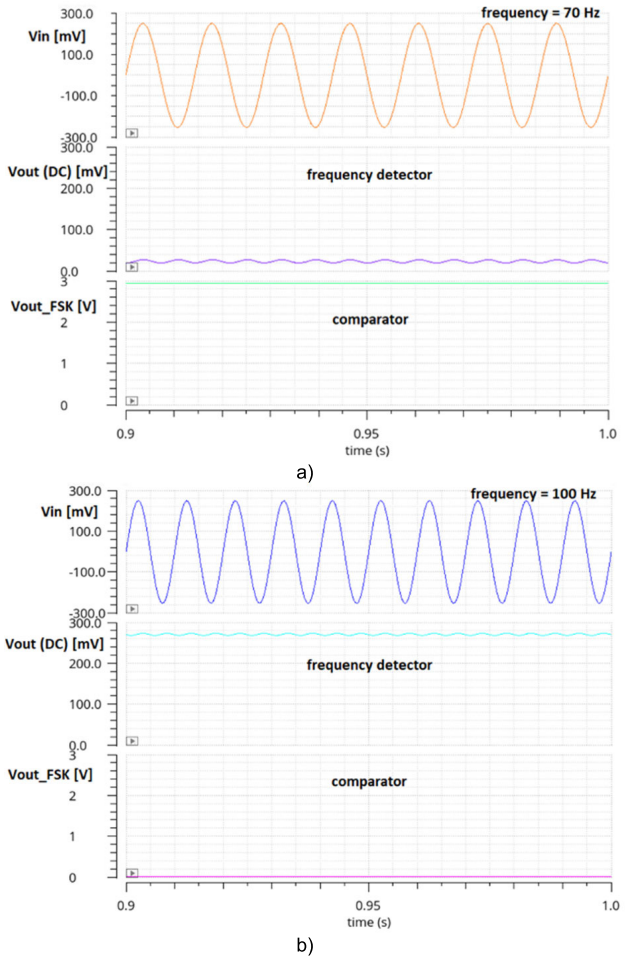

FIGURE 20. Simulated output response of signaling frequency detecting system of FSK demodulator (created by frequency detector and additional comparator) for input frequency: a) 70 Hz, b) 100 Hz.

transmitter. This application allows for us to detect specific frequency (f_p – where filter is adjusted). These distinctive features can be specified either by threshold distances (hysteresis window) of the comparator or by the slope (order, equivalent quality factor) of phase response of the iAP filter. Note that two-state demodulation (two signaling frequencies) requires two differently tuned and adjusted frequency detectors and comparators.

V. CONCLUSION

The presented concept of electronically reconfigurable filter offers a simple switchless reconfiguration of the transfer response (band-pass, inverting all-pass, special band reject and inverting direct transfer/attenuation) by a single parameter, typical for microwave structures, as well as simple electronic tuning of frequency. The proposed solution offers special transfer responses (by phase responses behavior) unavailable in standard concepts that can be beneficially utilized in further applications (adaptive frequency equalizers [46], random distortion level control [47], etc.).

Implementation of the FO resonator ensures stable operation where approximants of FO devices are connected in a grounded form. Further benefits of the implementation of the FO devices offer easy interchange of the attenuation slope of BP response by simple replacement of the FO device having different order. The circuit has high input and low output impedance. The design was specified for center frequency 100 Hz (fitting biomedical applications) and special transfer responses (phase response of sBR and iAP settings) show good agreement between theory, Cadence simulation and experimental results in the frequency band from 1 Hz up to 10 kHz. Tuning of the filter was tested between 10 and 100 Hz (the measured values are 10.7 Hz and 105 Hz).

Features of the filter predetermine application in slow ECG or EEG signal filtering and spectral modification (adaptive distortion removal [46], [47]) as well as various different purposes. Moreover, the AP/iAP responses serve as a general active delay line in many systems for communication and measurement purposes. The presented device can be used for phase/frequency detection or synchronization (alignment) of two signals with identical frequency and phase. The tested range of detection can be found around center frequency 100 Hz between 50 and 180 Hz (phase difference when input frequencies of multiplier are identical can be detected approximately between $\pm 100°$ in experimental case). The application example indicates operationability of phase/frequency detection in ten-hundreds of Hz. The maximal DC output voltage of phase/frequency detection reaches slightly more than 300 mV for alignment of waves, i.e. correspondence of input phase and frequency with set value of the filter in phase detector (100 Hz). The additional comparator together with frequency detector creates a frequency sensitive system evaluating the presence of specific frequencies for frequency shift keying demodulators or simple and precise (frequency resolution with higher accuracy than in filtering realized by a bank of filters) specific tone identification.

The presented design (theoretical idea) can be solved by different approaches and also by Field Programmable Analog Arrays (FPAAs) using different circuit topologies. Common designs using of-the-shelf (commercially available) active elements of building blocks in FPAA (standardly based on operational amplifiers) offer similar performance but the circuit and organization of passive and active elements will be more complex. It has different performances thanks to the available values and ranges (in selected way of design) of operation of fractional-order and active elements.

Theoretical concept of the system (circuit) can be created by commercially available analog devices. However, some transfer responses will not be available (e.g. for BP response when $A = 0$ or < 0, $g_m = 0$ or < 0 is unavailable in standard OTA). Standard OTAs do not provide a single bidirectional current output. Therefore, full operationability requires multiplier-based OTAs used in this work.

Limits of the proposed method (reconfigurability based on the sum of the response of resonator and branch of amplification) can be found in high dependence of the features of filter on accuracy of the equivalent value of CPEs and the quality of design of CPEs. Correct operation also requires special types of OTAs (based on multipliers) because zero value or positive and negative polarity of some transconductances

is required. The current design limits the tunability of the filter and operationability of frequency detecting application to tens-hundreds of Hz (especially by maximal value of g_m around 1 mS) but it is not a conceptual issue. It depends on the performances of active devices and features of CPEs that can be redesigned. The mentioned frequency range was set intentionally to slow operation following behavior of many natural biological [33] or communication systems [45].

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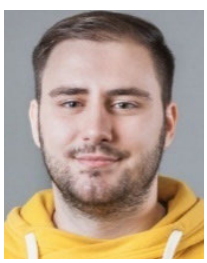

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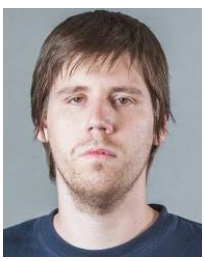

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Timeline and Summary of Other Publications with Contribution of the Author

4/2017 ***Special Electronically Reconfigurable Lossy/Lossless Integrator in Application of Functional Generator***

The paper deals with an idea of an electronically reconfigurable integrator utilized in nonlinear application of functional generator. Presentation was commenced during the proceedings at 27th International Conference Radioelektronika 2017.

Authors: Šotner, R.; Petržela, J.; Jeřábek, J.; Domanský, O.

4/2017 ***Desing Method Based on Modification of the Transformation of Horizontal Structures in Current-Mode Frequency Filters***

This paper presents a modification of the horizontal structure transformation method used for the design of fully-differential (F-D) filters. Proceedings of the 23nd Conference STUDENT EEICT 2017.

Authors: Langhammer, L.; Domanský, O.

6/2017 ***Synthesis and design of constant phase elements based on the multiplication of electronically controllable bilinear immittances in practice***

(impact factor: 3.169, Clarivate Analytics, 2023)

Presented work introduces a solution of new simplified two-active-elements-based bilinear immittance and investigates its implementation in loop of operational-transconductance-amplifiers-based impedance converter. The presented results show practical consequences of applying these bilinear immittance segments in CPE synthesis. The work was published in the journal AEU - International Journal of Electronics and Communications.

Authors: Šotner, R.; Jeřábek, J.; Petržela, J.; Domanský, O.; Tsirimokou, G.; Psychalinos, C.

6/2017 ***Single Active Parameter Tunable Simple Band-Pass Filter: Methods for Tunability Range Extension***

Lossless integrator implemented in the structure of the filter was solved as three different subcircuits allowing three different methods of its adjusting, i.e. linear, quadratic and exponential dependence of transconductance gm on DC driving voltage. Presented at Proceedings of the 24th International Conference "Mixed Design of Integrated Circuits and Systems".

Authors: Šotner, R.; Petržela, J.; Domanský, O.; Langhammer, L.; Dostál, T.

7/2017 ***Exponentially Tunable Voltage Controlled Quadrature Oscillator***

This paper deals with an appropriate method of tunability extension in quadrature oscillators. Exponential dependence of frequency of oscillations on the DC control voltage is created in lossless integrators by utilization of two exponentially controlled variable gain amplifiers and diamond transistors. The conference paper at the Proceedings of the 40th International Conference on Telecommunications and Signal Processing (TSP 2017).

Authors: Šotner, R.; Jeřábek, J.; Petržela, J.; Domanský, O.; Jaikla, W.; Dostál, T.

7/2017 ***A 1+α Low-Pass Fractional-Order Frequency Filter with Adjustable Parameters***

A novel solution of a fractional order low-pass type frequency filter is presented. The proposed structure comprises of two Double-Output Current Followers, two Multi-Output Current Followers and two Adjustable Current Amplifiers. Conference paper of Proceedings of 2017 40th International Conference on Telecommunications and Signal Processing (TSP 2017).

Authors: Langhammer, L.; Šotner, R.; Dvořák, J.; Domanský, O.; Jeřábek, J.; Uher, J.

9/2017 ***Current Feedback Operational Amplifier Based Two-Port Frequency Equalizer***

The paper brings a novel first-order bilinear two-port section (also called as a two-port block). The new topology reduces complexity and minimizes impact of fabrication dispersion (tolerances) of passive elements on transfer features. Paper was presented at the Proceedings of the 2017 23 European Conference on Circuit Theory and Design (ECCTD 2017).

Authors: Šotner, R.; Petržela, J.; Domanský, O.; Dostál, T.

4/2018 ***Electronically Reconfigurable Universal Filter Based on VDTAs***

The proposed filter extends features of the previously presented Voltage Differencing Transconductance Amplifiers (VDTAs)-based frequency filter. It brings the new advantage of an electronic reconfiguration of its transfer. The proposed paper was presented at the Proceedings of 28th International Conference Radioelektronika 2018.

Authors: Langhammer, L.; Šotner, R.; Domanský, O.; Hricko, T.

4/2018 ***Applications of novel behavioral implementation of a controllable generalized current conveyor***

This contribution presents a novel modification of a behavioral model for a generalized current conveyor of the second generation based on commercially available active devices. Presented at Proceedings of the 28th International Conference Radioelektronika 2018.

Authors: Šotner, R.; Langhammer, L.; Petržela, J.; Domanský, O.; Dostál, T.

7/2018

New Reconfigurable Universal SISO Biquad Filter Implemented by Advanced CMOS Active Elements

The proposed structure can be reconfigured to offer each of all five second-order transfers functions (high-pass, bandpass, low-pass, band-reject and all-pass) as well as setting of pole frequency and quality factor. Presented at Proceedings of the 2018 15th International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD).

Authors: Šotner, R.; Langhammer, L.; Domanský, O.; Petržela, J.; Jeřábek, J.; Dostál, T.

9/2018

Reconnection-less Reconfigurable Filter and its Application into Adaptive Circuit

A special topology of a reconnection-less reconfigurable second-order filter. Its features of available transfer functions are unique because none of the previously reported solutions provides similar features. Our concept is easily implementable thanks to the simple commercial active devices as shown in the paper. Presented at the Proceedings of the IEEE 2018 41st International Conference on Telecommunications and Signal Processing (TSP 2018).

Authors: Šotner, R.; Jeřábek, J.; Petržela, J.; Langhammer, L.; Domanský, O.; Jaikla, W.; Dostál, T.

11/2018

Practical Design of Fractional-Order Oscillator Employing Simple Resonator and Negative Resistor

This contribution presents a straightforward design of a fractional-order oscillator employing a novel simple impedance inverter (implementing a differential voltage current conveyor transconductance amplifier as an active element) used for a construction of a parallel LC resonator. Proceedings of the 10th IEEE International Congress on Ultra Modern Telecommunications and Control Systems (ICUMT 2018).

Authors: Šotner, R.; Jeřábek, J.; Domanský, O.; Herencsár, N.; Kartci, A.; Dvořák, J.

3/2019

Electronically reconfigurable two-path fractional-order PI/D controller employing constant phase blocks based on bilinear segments using CMOS modified current differencing unit

(impact factor: 1.992, Clarivate Analytics, 2023)

This work introduces a versatile type of electronically controllable bilinear transfer segments, i.e. two ports allowing an independent electronic control of zero and pole of transfer function, based on a modified current differencing unit (MCDU) an active element as a part of a novel two-path system of the fractional-order proportional-integral or a derivative (FOPI/D) controller. The solution was published in Microelectronics Journal.

Authors: Šotner, R.; Jeřábek, J.; Kartci, A.; Domanský, O.; Herencsár, N.; Kledrowetz, V.; Alagoz, B.; Yeroglu, C.

7/2019 ***Simple Chaotic Oscillator with Wideband Passive Fractional-Order Inductor***

The solution demonstrates through computer-aided simulations that simple loop composed of single nonlinear active two-port and a fractional-order filter can generate robust chaotic attractor. Presented at Proceedings of 42nd International Conference on Telecommunications and Signal Processing (TSP 2020).

Authors: Petržela, J.; Domanský, O.

10/2019 ***Electronically Tunable Oscillator Utilizing Reinforced Controllable Parameters***

A novel solution of an oscillator with electronically adjustable oscillation condition and frequency of oscillations. An oscillation condition is controlled by current gain and frequency of oscillations is adjustable by transconductance. Presented at Proceedings of the 2019 11th International Congress on Ultra Modern Telecommunications and Control Systems and Workshops (ICUMT 2019).

Authors: Langhammer, L.; Šotner, R.; Domanský, O.

4/2020 ***Comparison of Simple Design Methods for Voltage Controllable Resistance***

The paper compares several ways of electronic resistance control for tunable applications (filters, oscillators, amplifiers, etc.). Simulation (PSpice) and experimental tests of a basic J-FET transistor-based adjustable resistor. Presented at the Proceedings of 30th International Conference Radioelektronika.

Authors: Šotner, R.; Domanský, O.; Langhammer, L.; Petržela, J.

Legend: - journal article; - conference paper

- main authorship; - second author

F Design Method Based on Modification of the Transformation of Horizontal Structures in Current-Mode Frequency Filters

Outline

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Author's Contribution

The author took part in performing the analysis and wrote a part of the manuscript and helped to ensure reviewing and editing.

Author's contribution: 25 % (the second author).

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DESIGN METHOD BASED ON MODIFICATION OF THE TRANSFORMATION OF HORIZONTAL STRUCTURES IN CURRENT-MODE FREQUENCY FILTERS

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Abstract: This paper presents a modification of the horizontal structures transformation method used for the design of fully-differential (F-D) filters. The modified method has been tested on numerous filtering structures based on current followers (CF) and chosen results are included in the paper proving its functionality

Keywords: design method, frequency filters, transformation of horizontal structures

1. INTRODUCTION

A demand for better characteristics of filtering structures has been increased in recent years. The proposal of fully-differential filters [1-3] seems to be one of the promising area of research in this field. Differential signal processing is a part in many industrial fields such as data transmission, audio-electronics, instrumentation, etc. thanks to its immunity to external interference. Except the ability to suppress the common-mode signals, the fully-differential structures perform better power supply rejection ratio, greater dynamic range of the processed signals and lower harmonic distortion [1].

There are many ways how to propose single-ended (S-E) frequency filters. We can mention the way using autonomous circuit design method [4], synthetic immittance system method [5], signal-flow graphs (SFGs) method [6], etc. The literature describes three possible ways used for the design of fully-differential (F-D) filters. The first one is a direct proposal of a F-D filter [7]. However, this approach requires an experienced designer and the proposal can be time-consuming. The second method implements the coupling of S-E filters [8-9] connected together through a common node which is not connected to the ground. The resulting structures obtained by this method offer high Common Mode Rejection Ratio (CMRR). The drawback of this method is the fact that the resulting filter has approximately twice of the passive (RC) elements than S-E structure and it also may consist floating capacitors (unsuitable for the integration). The last method focuses on the transformation of the S-E structure into the F-D structure by "mirroring" of passive parts around the horizontal axis of the structure [10], [11]. Unfortunately, the number of passive components increases approximately two times in comparison to the number of passive parts contained in the S-E structure. This method can be easily implemented and the number of used active elements remain the same when replacing the S-E active elements by their F-D equivalents. The tradeoff of this way leads to lower CMRR [8].

The last discussed design method can be divided into the transformation of vertical structures and transformation of horizontal structures [12]. Our improved proposal belongs to transformation of horizontal structures. Therefore, this type of transformation will be explained in further text. This transformation involves the mirroring of passive parts of the horizontal branches of the initial S-E circuit structure. The values and positions of passive parts, included in vertical braches, remain

unchanged when the values of the horizontal parts are modified in dependence on the specific type of used passive element. The values of capacitors are doubled, while the values of resistors are halved. Inductors are replaced by transformers with mutually opposite winding when the number of windings is even.

2. MODIFICATION OF THE HORIZONTAL STRUCTURES TRANSFORMATION METHOD

This modified design method is supposed to be implemented in current-mode frequency filters based on current followers (CF). The design procedure is explained on the transformation of a lossless integrator depicted in Fig. 1a). In order to transform the S-E structure from Fig. 1a) into a corresponding F-D structure using the transformation of horizontal structures, the passive components placed in the horizontal branches of the circuit are mirrored and their values transform as explained above (conductance *G* is mirrored around the CF and now having value of 2*G*). The value and position of the capacitor *C* preserves unchanged. The resulting structure is shown in Fig. 1b). However, originally grounded capacitor *C* turns into a floating capacitor which is not suitable for the integration. This capacitor must be then replaced by two grounded capacitors (one for each branch of the F-D structure) as illustrated in Fig. 1c). Note that the transformation of the horizontal structures (explanation in literature [12]) does not include this additional step of the design. The values of the grounded capacitors (Fig. 1c), given in the F-D structure, must reach two-times higher value than capacitor used in the S-E structure due to the doubled values of horizontal parts in order to obtain the same pole frequency of transfer function of both mentioned structures.

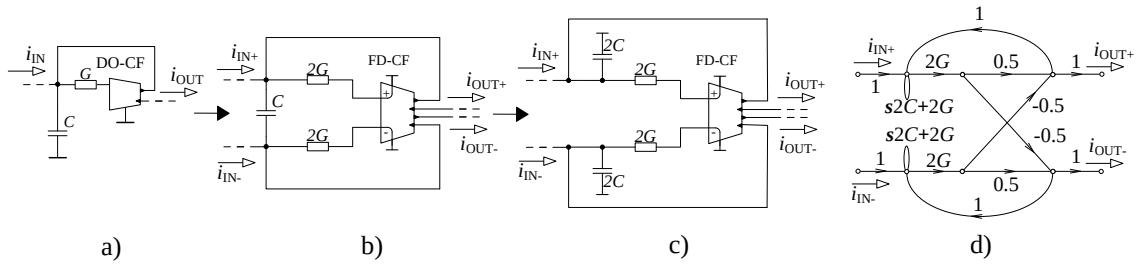

Figure 1: Design steps: a) initial S-E structure, b) the resulting F-D structure created by the transformation of horizontal structures, c) the resulting F-D structure with grounded capacitors, d) corresponding simplified M-C graph

Figure 2 illustrates the transformation of the same S-E structure as presented in Fig. 1a) using the modified method. The modified method considers the grounded capacitors contained in the F-D structure as starting point of the proposal. Therefore, the values of resistors (conductances *G*) and capacitors *C* of the F-D structure stay the same as values of passive parts of the S-E structure as shown in Fig. 2b).

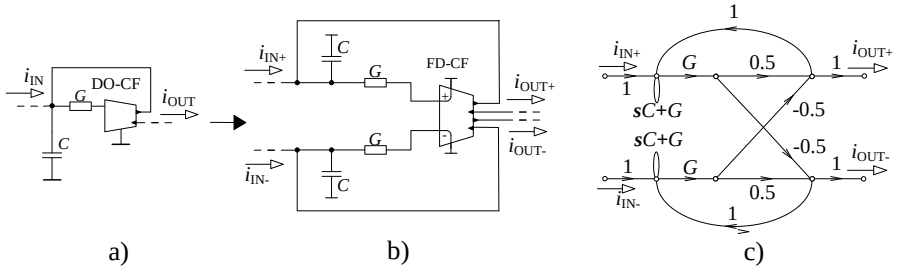

Figure 2: Design steps: a) initial S-E structure, b) the resulting F-D structure created by the modified design method, c) corresponding simplified M-C graph

Figure 1d) and Fig. 2c) show the Mason-Coates (M-C) graph of the F-D structure from Fig. 1c), Fig. 2b) respectively. The identical result of symbolical transfer function and behavior of F-D structures in Fig. 2b and Fig. 1c (while circuit in Fig. 2b employs half of values of passive

elements than in Fig. 1c) is supported by following mathematical derivation. These calculations are based on the SFG method using the Mason gain formula.

The denominator of transfer function of the simplified M-C graph from Fig. 1d) is given by:

$$\begin{aligned} D(\boldsymbol{s}) &= (\boldsymbol{s}2C + 2G)\cdot(\boldsymbol{s}2C + 2G) - (0.5\cdot 2G\cdot(\boldsymbol{s}2C + 2G)) - \\ &- (0.5\cdot 2G\cdot(\boldsymbol{s}2C + 2G)) - (-0.5\cdot(-0.5)\cdot 2G\cdot 2G) + \\ &+ 0.5\cdot 0.5\cdot 2G\cdot 2G = 4\boldsymbol{s}^2C^2 + 4\boldsymbol{s}CG + 4\boldsymbol{s}CG + 4G^2 - 2\boldsymbol{s}CG - \\ &- 2G^2 - 2\boldsymbol{s}CG - 2G^2 - G^2 + G^2 = 4\boldsymbol{s}^2C^2 + 4\boldsymbol{s}CG. \end{aligned} \quad (1)$$

The numerator of the given M-C graph is equal to:

$$N(\boldsymbol{s}) = 4\boldsymbol{s}CG + 4G^2. \quad (2)$$

As can be seen all terms of the denominator and numerator contain "4" which will cancel each other and the transfer function of the F-D structure from Fig. 1c) is given by:

$$K(\boldsymbol{s}) = \frac{I_{OUT+} - I_{OUT-}}{I_{IN+} - I_{IN-}} = \frac{\boldsymbol{s}CG + G^2}{\boldsymbol{s}^2C^2 + \boldsymbol{s}CG} = \frac{G}{\boldsymbol{s}C}. \quad (3)$$

The denominator of transfer function of the simplified M-C graph from Fig. 2c) is calculated as:

$$\begin{aligned} D(\boldsymbol{s}) &= (\boldsymbol{s}C + G)\cdot(\boldsymbol{s}C + G) - (0.5\cdot G\cdot(\boldsymbol{s}C + G)) - (0.5\cdot G\cdot(\boldsymbol{s}C + G)) - \\ &- (-0.5\cdot -0.5\cdot G\cdot G) + 0.5\cdot 0.5\cdot G\cdot G = \boldsymbol{s}^2C^2 + \boldsymbol{s}CG + \boldsymbol{s}CG + G^2 - 0.5\boldsymbol{s}CG. \\ &- 0.5G^2 - 0.5\boldsymbol{s}CG - 0.5G^2 - 0.25G^2 + 0.25G^2 = \boldsymbol{s}^2C^2 + sCG. \end{aligned} \quad (4)$$

The numerator of the corresponding M-C graph is given by:

$$N(\boldsymbol{s}) = \boldsymbol{s}CG + G^2. \quad (5)$$

Thus, the resulting transfer of the F-D structure from Fig. 2b) is given as:

$$K(\boldsymbol{s}) = \frac{I_{OUT+} - I_{OUT-}}{I_{IN+} - I_{IN-}} = \frac{\boldsymbol{s}CG + G^2}{\boldsymbol{s}^2C^2 + \boldsymbol{s}CG} = \frac{G}{\boldsymbol{s}C}. \quad (6)$$

The equation (3) describes the resulting transfer function of the F-D structure which has been created by the transformation of the horizontal structures. The equation (6) denotes the resulting transfer function of the F-D structure based on the modified transformation method. Both equations are identical. Therefore, the modified design method can be used instead of the transformation of horizontal structure.

3. SIMULATIONS AND RESULTS

Figure 3 shows several results of simulations of band-pass filter (BP) which is taken from [13] as well as the values of all passive elements and parameters. The initial S-E transfer function (Figure 1a)) is represented by blue line in Fig. 3. The green line visualizes the F-D transfer function (Figure 1b)) created by transformation of S-E function where horizontal conductance *G* was replaced by two horizontal conductances *2G* and by one floating capacitor *C*. The purple dot line indicates modified F- D structure where floating capacitor *C* was transformed into two grounded capacitors *2C* (having value of the original floating capacitor). The construction based on new modified method discussed in previous chapters results in simulated trace distinguished by the red line. The transfer function obtained by the modified method almost follows original S-E function and at lower frequencies (up to 10^4 Hz) achieves better attenuation, in the whole decade, than F-D horizontal floating structure.

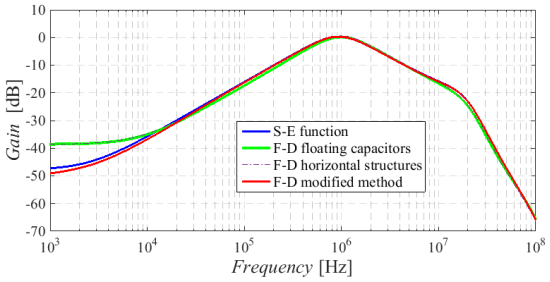

Figure 3: Comparison of BP simulated S-E and F-D transfer functions

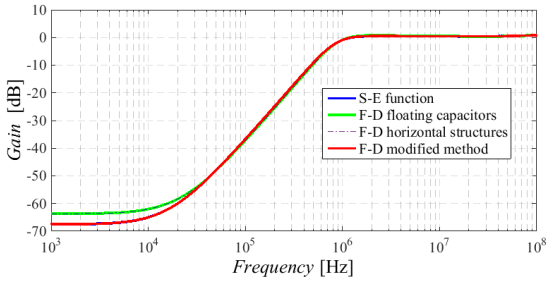

Figure 4: Comparison of HP simulated S-E and F-D transfer functions

Figure 4 is the comparison of HP transfer function of the filter from [14]. As in previous case modified F-D method (red line) offers better results than F-D method with floating capacitor (green line) as well as F-D method with horizontal structure (purple dot line).

The simulation results presented in Fig. 3 and Fig. 4 are carried out using a 3rd level simulation model of the UCC (closely described in [15]) and 3rd level simulation model of the DACA (presented in [16]). These models include the frequency depended imitation of impedances of input and output terminals of given active elements alongside with current limitations of individual inputs and outputs.

4. CONCLUSION

The proposed method is based on the transformation of the design method for horizontal filtering structures which was modified in accordance to the specific requirements and characteristics of differential structures. The validity and operation of the modified method was proved mathematically and supported by simulations. The obtained results are subsequently compared with results gained from method dealing with transformation of the horizontal structures.

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G Simple Chaotic Oscillator with Wideband Passive Fractional-Order Inductor

Outline

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The author helped to co-authorship of the validation of results and simulations as well as preparation of the presentation at TSP conference.

Author's contribution: 20 % (the second author).

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Simple Chaotic Oscillator with Wideband Passive Fractional-Order Inductor

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***Abstract*—This paper demonstrates through computer-aided simulations that simple loop composed of single nonlinear active two-port and a fractional-order filter can generate robust chaotic attractor. Involved passive ladder trans-impedance mode filter contains two-terminal constant phase element that is accurately approximated in the frequency domain in wide frequency range; beginning at 10 Hz and ending with 1 MHz. It is shown that the mathematical order of a designed lumped chaotic system can be decreased significantly below 3 without qualitative changes in the global dynamics. Fundamental properties of the filtering network responsible for chaos evolution are specified and discussed.**

***Keywords*—chaos theory; fractional-order inductor; laplace transform; nonlinear dynamics; oscillator; strange attractors; trans-immittance; transfer function**

I. Introduction

Construction of chaotic oscillators becomes a favorite topic of design engineers since discovery and description of the first very simple autonomous deterministic electronic circuit that exhibits robust chaotic behavior [1, 2]. This kind of oscillator was discovered by Prof. L. O. Chua and can generate a dense bounded state attractor with the non-integer metric dimension. Generally speaking, circuit synthesis leading to the fully analog chaotic oscillator is a simple and straightforward process [3] especially if the covering mathematical model is known. Thus, implementation of individual analog building blocks as well as whole chaotic system on a single chip using unified fabrication process is nothing than one logical step further [4]. Sampling of continuous-time signals for a digital realization of complicated nonlinear transfer functions represents changes in mathematical model. However, global behavior can be still preserved [5].

Basically, there are two mechanisms simultaneously acting in a vector field that are responsible for evolution of the chaotic dynamics. First one is called stretching and causes exponential divergence (separation) of two neighboring state trajectories. Second one eventually folds state orbit to make the ω-limit set bounded. Because of the consequences coming from Poincaré-Bendixon´s theorem the isolated dynamical system must have at least three degrees of freedom to exhibit true chaotic nature. For deterministic dynamical systems periodically driven by one or several external energy sources chaos can be observed in the case of second-order internal dynamics [6] and higher.

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Recently, a fractional-order (FO) calculus [7, 8] enters also research area of mathematical modeling and nonlinear system analysis. It is generally assumed that FO dynamical system is more accurate in task of modeling real physical, technical and environmental phenomenon. In the case of the specific chaotic systems, it turns out that one or several describing ordinary differential equations could be considered with the non-integer real-valued order between zero and one while desired strange attractor remains robust and observable both numerically and experimentally, i.e. chaos is not a transient motion.

So far, FO lumped chaotic circuits were mostly constructed using well-established conception of the analog computers. FO element used here is designed in the form of inverting voltage integrators where feedback capacitor is replaced by few passive series-parallel RC sections. There are two serious drawbacks of this approach. Firstly, many RC sections need to be used if wideband chaotic signals with continuous frequency spectrum are involved. Unfortunately, this is common error overlooked in many papers. Secondly, final oscillators are too complicated with necessity to utilize many active as well as passive circuit components. Upcoming sections of this brief paper study very simple oscillator´s configuration where a conventional inductor is replaced by FO two-terminal passive linear equivalent.

II. Configuration of Chaotic Oscillator

Searching for the canonical circuitry realization of a chaotic oscillator starts with finding a convenient algebraically simple mathematical model. Jerky dynamics, i.e. a single higher-order ordinary differential equation, seems to be a good candidate.

Let suppose that nonlinear active two-port works in trans-admittance mode, i.e. as voltage-controlled current-source [9]. Thus, in order to close loop of two blocks, filter needs to work in a complementary, trans-impedance mode $Z_t(s)=V_{out}/I_{in}$. This trans-impedance can be expresses in Laplace transform as

$$Z_t(s)=\frac{1}{C_1C_2E\cdot s^{2+\alpha}+\frac{C_1E}{R}s^{1+\alpha}+\frac{C_1+C_2}{E}s+\frac{1}{R}}, \quad (1)$$

where E is constant in $s^{1-\alpha}/F$ defined as value of module at the singular frequency 1 rad/s.

Proposed novel chaotic oscillator with single FO element is provided by means of Fig. 1. Note that, excluding realization of FO element, a designed oscillator contains only one active and four passive components. Dynamics of this network is uniquely described by a following mathematical model

$$C_1\frac{d}{dt}v_1 = -\frac{v_1}{R} - i_E + \frac{K}{R_x}v_2(v_2 - V_{ext})$$
$$C_2\frac{d}{dt}v_2 = i_E \qquad E\frac{d^\alpha}{dt^\alpha}i_E = v_1 - v_2 \qquad (2)$$

where a state vector is $\mathbf{x}=(v_1, v_2, i_E)^T$, K=0.1 represents internal constant of four-quadrant analog multiplier AD633 and the real number $\alpha \in (0, 1)$ stands for a decimal order of last differential equation. As prototype of integer-order chaotic system, we can adopt the following values C_1=5.7 nF, C_2=1 nF, L=700 mH and R_x=2 kΩ. Remaining resistor R changes; larger values of this resistor need to be used for a decreased mathematical order α. For α=1 this resistor will be R=7.7 kΩ. Preliminary numerical analysis of dynamical system (2) for order α=1 is provided by means of Fig. 2. State trajectories presented here were obtained using Mathcad and a build-in fourth order Runge-Kutta method with fixed time step 10 μs and final time 100 ms.

III. Design of FO Two-Terminal Device

After years of intensive experimentation with FO circuits in different applications (such as frequency filters, phase shifters, oscillators, feedback controllers and PID regulators) it seems that the best way how to realize a FO circuit element dedicated for useful signal frequencies up to tens of MHz is thoroughly described in [10, 11] including numerical routine how to obtain values of passive circuit components. It also means that a fully passive ladder circuitry realization of FO circuit element has superior properties over existing active implementation that are based on ideal cascade synthesis: using standard bilinear filters [12, 13], electronically adjustable first-order filtering sections [14, 15] or band-reject biquadratic filters [16]. Approach [11] represents approximation of ideal FO element in the frequency domain by a complex two-terminal immittance function having real zeroes and poles. These zeroes and poles alternate on a real (frequency) axis of complex plane and create a phase response rippled around some predefined ideal value.

For α=0.9, that is a phase shift between voltage and current 81°, we can utilize serial connection of L_s=330 mH and R_s=4 Ω and seven series-parallel combinations R_1=20 Ω, L_1=200 mH, R_2=105 Ω, L_2=170 mH, R_3=556 Ω, L_3=140 mH, R_4=2860 Ω, L_4=120 mH, R_5=14750 Ω, L_5=97 mH, R_6=77 kΩ, L_6=80 mH, R_7=400 kΩ and L_7=67 mH. In this case, numerical value of the fundamental constant E is 8.596 $s^{0.1}$/F.

For α=0.8, that is a phase shift between voltage and current 72°, we can use serial combination of L_s=150 mH and R_s=15 Ω and seven series sub-blocks R_1=60 Ω, L_1=600 mH, R_2=256 Ω, L_2=418 mH, R_3=1100 Ω, L_3=285 mH, R_4=5 kΩ, L_4=200 mH, R_5=21 kΩ, L_5=137 mH, R_6=91 kΩ, L_6=95 mH, R_7=400 kΩ and L_7=75 mH. Numerical value of constant E is 19.605 $s^{0.2}$/F.

For α=0.7, i.e. for phase shift of FO impedance 63°, we can use serial connection of L_s=21.6 mH and R_s=14 Ω and seven series-parallel combinations R_1=45 Ω, L_1=450 mH, R_2=164 Ω, L_2=252 mH, R_3=581 Ω, L_3=155 mH, R_4=2100 Ω, L_4=86 mH, R_5=7400 Ω, L_5=50 mH, R_6=27200 Ω, L_6=29 mH, R_7=100 kΩ and L_7=18 mH. Numerical value of constant E is 15.678 $s^{0.3}$/F.

For α=0.6, that is for phase shift of FO impedance 54°, we can use following values L_s=2.5 mH and R_s=9 Ω in cooperation with seven series-parallel combinations R_1=22 Ω, L_1=219 mH, R_2=67 Ω, L_2=105 mH, R_3=200 Ω, L_3=50 mH, R_4=588 Ω, L_4=24 mH, R_5=1700 Ω, L_5=11.6 mH, R_6=5.3 kΩ, L_6=5.5 mH, R_7=16100 Ω and L_7=3.1 mH. Numerical value of fundamental constant associated with FO inductor E is 9.468 $s^{0.4}$/F.

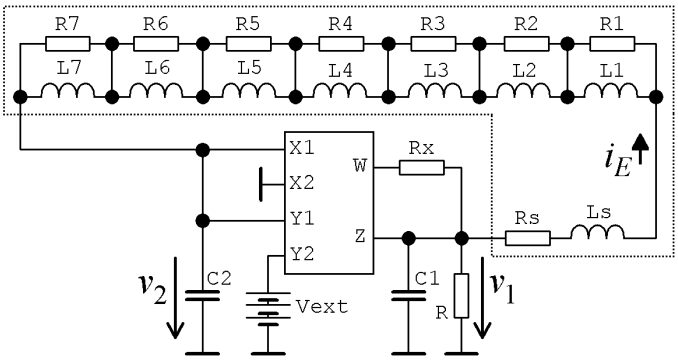

Fig. 1. New concept of the simple fully analog chaotic system with general realization of FO passive floating inductor (situated inside a dotted area).

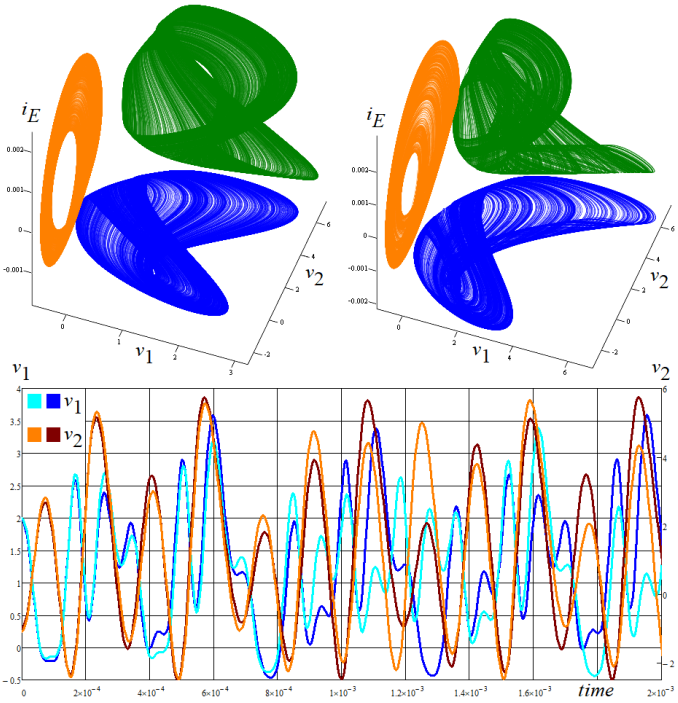

Fig. 2. Three-dimensional visualization of the numerically integrated typical strange attractor generated by the integer-order prototype of proposed chaotic system (upper plots): v_1 vs v_2 plane (blue), v_1 vs i_E plane (green) and v_2 vs i_E plane (orange) for V_{ext}=2.9 V (left) and V_{ext}=3.4 V (right). Chaotic signals v_1 and v_2 in the time domain (lower graph). Individual pairs of the waveforms demonstrate sensitivity of a dynamical system (2) to tiny changes in the initial conditions: light blue and orange traces have initial state $\mathbf{x}_0=(2, 0.03, 0)^T$ while dark blue and brown trajectories have initial state $\mathbf{x}_0=(2, 0.031, 0)^T$.

For α=0.5, i.e. for phase shift of FO impedance 45°, we can use serial connection of L_s=0.73 mH and R_s=20 Ω and seven combinations R_1=36 Ω, L_1=348 mH, R_2=87 Ω, L_2=140 mH, R_3=217 Ω, L_3=56 mH, R_4=541 Ω, L_4=22.3 mH, R_5=1370 Ω, L_5=9 mH, R_6=3800 Ω, L_6=3.7 mH, R_7=10 kΩ and L_7=1.4 mH. Because of its dynamics this FO element can be marked as the passive half-inductor. In this case, numerical value of the fundamental constant E is 20.469 $s^{0.5}$/F.

Control Orcad Pspice based analysis of the constructed FO two-terminal devices is shown in Fig. 3. Note that, as requested by a "chaotic" application, approximation for all orders is valid in a wide frequency range starting with 10 Hz and ending with 1 MHz. Designed passive FO approximants are quite accurate; a maximal phase error in above-mentioned frequency range is less than 1.5° and relative error is less than 1% in a quite large middle part of frequency operational range (100 Hz to 30 kHz). For better clarification see visualization provided in Fig. 4.

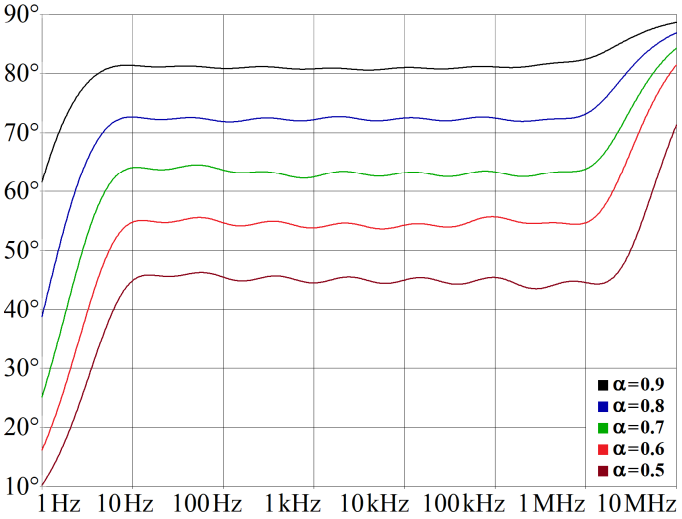

Fig. 3. Phase frequency responses of designed FO two-terminal devices used for the computer-aided verification of the proposed chaotic electronic system, theoretical value is flat with a constant value 90α°.

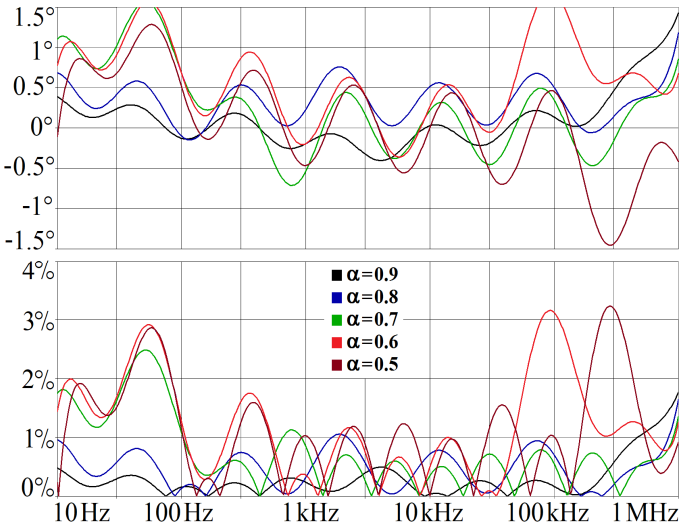

Fig. 4. Phase difference between ideal FO inductor and its approximation for different decimal orders (upper graph) and frequency dependence of a relative error expressed in % (lower plot).

However, such phase precision will be seriously violated if inductors and resistors will be subjects of fabrication tolerances and similar imperfections. Figure 5 shows that phase difference between real and ideal (flat) value can raise up to 3° (especially for order α=0.6) if very small 0.2% tolerances of inductors are considered. Note that maximal phase error double. Such large errors make FO approximant useless for many practical signal processing applications. Thus, FO approximants in general needs to be constructed very carefully and by using measured passive circuit components. These plots demonstrate 1000 runs with random generation of the circuit parameters with uniform distribution were used.

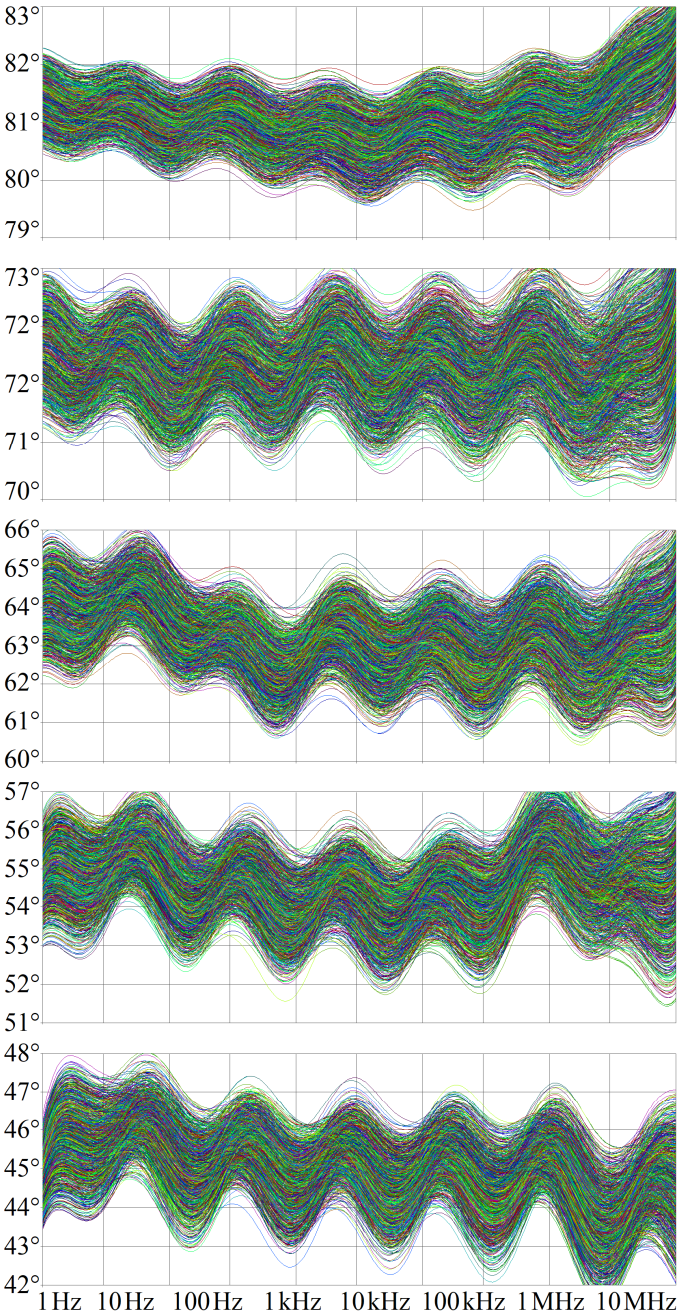

Fig. 5. Orcad Pspice based Monte Carlo analysis applied on constructed passive FO two-terminal elements; small but achievable 0.2% tolerance (normal distribution) of each inductor is assumed.

IV. Orcad Pspice Verification of FO Chaotic System

Chaotic circuit provided in Fig. 1 with passive two-terminal FO elements with different mathematical orders was verified by the computer-aided analysis. Basic parameters of simulation profile of Orcad Pspice program was fixed to final time 300 ms and maximum step size 1 µs.

Figure 6 shows Monge projections of the typical strange attractor generated by network with α=1. Figure 7 provides us with the same kind of results but for order α decreased to value 0.9. Simultaneously, also system dissipation was significantly lowered by increasing resistance R=50 kΩ. Note that generated strange attractor is slightly different. For both cases mentioned above external voltage was set to V_{ext}=3.4 V. Experimentation shows that mathematical order can be further lowered but with the cost of raised external DC voltage. FO element with α=0.8 approximation can be used for chaos generation if V_{ext}=5 V and R=200 kΩ, see Fig. 8. For order α=0.7 strange attractor can be observed if the external voltage V_{ext}=10 V, resistor being raised to R=500 kΩ and R_x=1.2 kΩ, consult graphical output in Fig. 9.

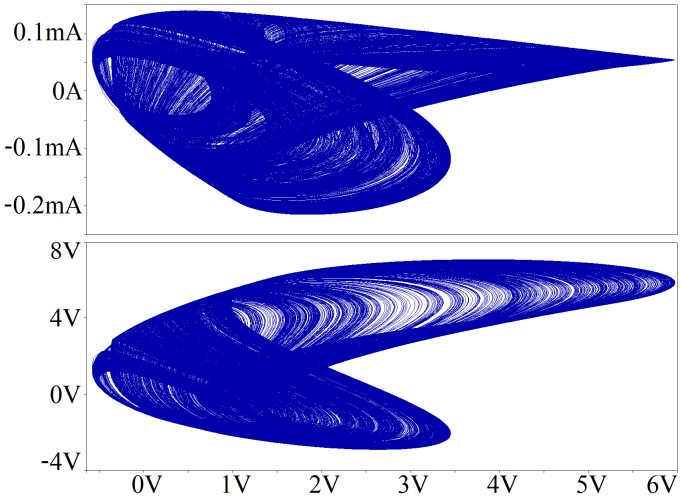

Fig. 6. Circuit simulation results for the integer-order prototype of a chaotic oscillator: v_1 vs i_E plane projection (upper plot) and v_1 vs v_2 plane (lower plot).

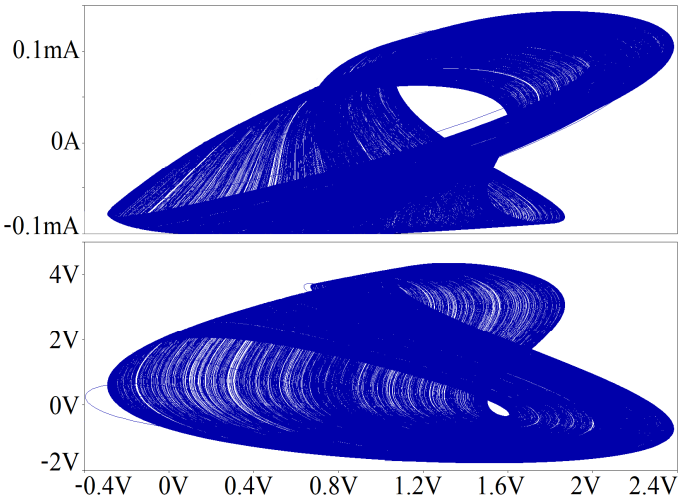

Fig. 7. Circuit simulation results for a chaotic oscillator in configuration with FO α=0.9: v_1 vs i_E plane projection (upper plot), v_1 vs v_2 plane (lower plot).

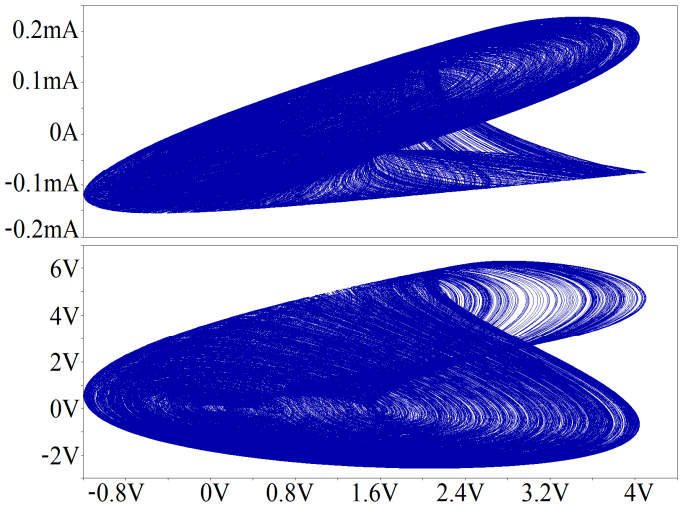

Fig. 8. Circuit simulation result for chaotic oscillator with total mathematical order 2.8 (α=0.8): v_1 vs i_E projection (upper plot), v_1 vs v_2 plane (lower plot).

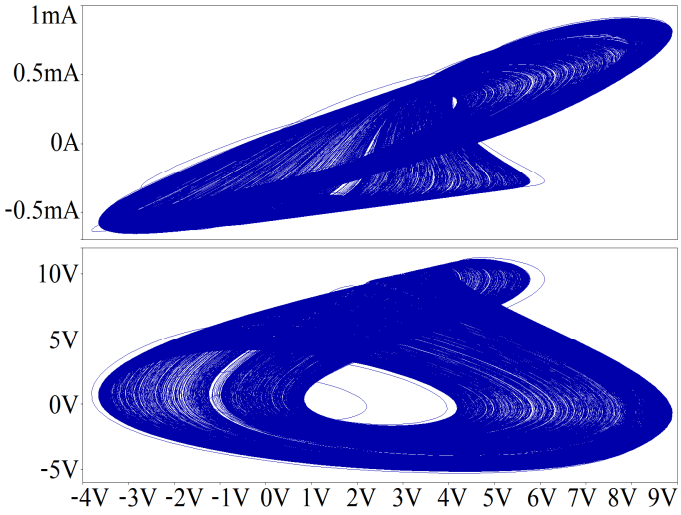

Fig. 9. Circuit simulation results for order α=0.7 of designed chaotic system: v_1 vs i_E plane projection (upper plot) and v_1 vs v_2 plane (lower plot).

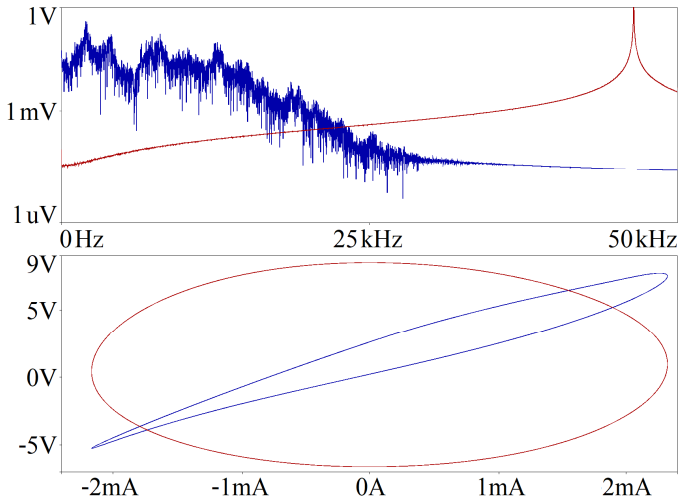

Fig. 10. Comparison between frequency components of a signal generated by oscillator with α=1 (blue) and α=0.6 (red), plane projections of limit cycle.

Unfortunately, it turns finally out that chaotic orbit cannot be generated by FO circuit having the lower order. Figure 10 shows that the chaotic nature disappears, and dynamical system starts to exhibit periodic solution. If approximated order α=0.6 is used with external voltage V_{ext}=10 V, resistor R=300 kΩ and R_x=600 Ω, corresponding graphical visualization is shown by means of Fig. 10. Note that, for constructed CPE, frequency of self-oscillation is about 45 kHz, i.e. value much higher than the highest significant frequency of a chaotic waveform generated by the original integer-order chaotic circuit.

There is a strong reason to believe that used passive ladder FO filter can be interchanged by arbitrary two-port structure (including active realizations) with a complex trans-immittance transfer function equivalent to module frequency characteristic

$$\left|1/Z_t(j\omega)\right| = \sqrt{\left[\frac{1}{R} - C_1C_2E\omega^{2+\alpha}A - \frac{C_1E}{R}\omega^{1+\alpha}B\right]^2 + \left[\frac{C_1E}{R}\omega^{1+\alpha}A + \frac{C_1+C_2}{E}\omega - C_1C_2E\omega^{2+\alpha}B\right]^2}, \quad (3)$$

with order-dependent constants A=cos($\alpha\pi$/2) and B=sin($\alpha\pi$/2). Finding suitable passive filter with only resistors and capacitors could be interesting topic for future investigations.

V. Conclusion

This paper demonstrates that the structurally stable strange attractors can be observed in a very simple autonomous chaotic oscillator with a mathematical order less than three. Chaotic nature of the generated waveforms is proved and quantified by positive largest Lyapunov exponent; this exponent is extracted from sequence of time-domain data. It turns out that total order can be decreased to value 2.7 but not further. Thus, total circuit order seems to be additional degree of freedom that can be used for the control of chaos. Designed chaotic oscillators are also suitable for true practical experiments if FO approximant are implemented precisely.

Further research in this area, that is lowering mathematical order of chaotic oscillator, can be conducted by substitution of standard capacitors by FO immittance equivalents [17]. Such substitution can give rise to interesting dense strange attractors; if either isolated [18, 19] or non-autonomous [20, 21] nonlinear dynamical systems are considered.

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H Comparison of Simple Design Methods for Voltage Controllable Resistance

Outline

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Author's Contribution

The methodology and consultations of the final simulation design, visualization and data processing.

Author's contribution: 15 % (the second author).

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Comparison of Simple Design Methods for Voltage Controllable Resistance

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***Abstract*—This paper compares several ways of electronic resistance control for tunable applications (filters, oscillators, amplifiers, etc.). Simulation (PSpice) and experimental tests of basic J-FET transistor-based adjustable resistor, optocoupler as well as more advanced active solutions using active devices (variable gain amplifiers, voltage-mode multiplier) are performed in order to see available linear range, readjustability range and expected frequency features.**

Keywords— Electronic control, J-FET, resistor, variable gain amplifier, voltage driving

I. Introduction

Integrated circuit design [1] offers very easy way of adjustability in applications depending on resistor value(s). Especially very simple construction of operational transconductance amplifier (OTA) [2]-[4] and its simple application for resistor emulation [2] represents the main benefit of this way. However, standard constructers and designers have quite limited possibilities. There are several ways including also discontinuously settable digital potentiometers [5], [6] or digital to audio converters [7]. Unfortunately, many analog and mixed applications and systems require continuous adjustability of resistance value where these solutions are not suitable. The continuous control of resistance value, solved by analog way, has certain limitations. The highest issues are linearity of voltage dependence across the element on current and frequency bandwidth limitation. Standard component base, available for designers, offers several types of J-FET and MOSFET transistors [8], that can be used for resistor replacement (operating in linear/triode regime [1], [8]) but also some special types of electronically adjustable active elements can be selected as better option for indicated features (resistivity control in circuit application with operational amplifiers for example).

The following text compares several typical and also unusual ways of electronic control of resistance and compares their linearity, range of applied current and voltage across the element, frequency bandwidth and range of available resistance value.

II. Easily Available Methods of Resistance Control

A. Single J-FET transistor

The simplest method of replacement of resistor by electronically adjustable equivalent supposes usability of MOSFET transistor [1], [8] in triode/linear (ohmic regime). The method is very simple and straightforward but result has several important drawbacks and limitations discussed in experimental part. The basic circuits using depletion Junction FET (J-FET) [8] of N channel polarity are shown in Fig. 1. The driving voltage V_{set} has negative polarity for this type of transistor. Large signal analysis of circuit in Fig. 1(a) determines equivalent resistance of JFET in form ($V_{GS(off)}$ is threshold voltage and I_{DSS} is maximal drain short channel current for zero bias):

$$R_{eq\_large} = \frac{V_{GS(off)}}{I_{DSS}\left[\left(V_{GS}-V_{GS(off)}\right)-\frac{V_{DS}}{2}\right]}. \quad (1)$$

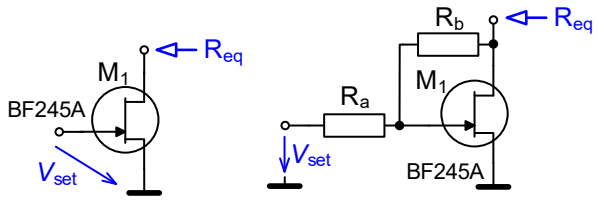
Small-signal resistance (for $V_{DS} < V_{GS} - V_{TH}$) is defined as:

$$R_{eq\_small} = \frac{V_{GS(off)}}{I_{DSS}\left(V_{GS}-V_{GS(off)}\right)}, \quad (2)$$

unfortunately, nonlinearity of this solution for larger V_{DS} voltages is high (usability up to tens of mV and low tens-hundreds of μA), therefore Senani et al. [9], [10] presented improved version using resistor divider in Fig. 1(b) (having equal resistances) in order to reduce influence of V_{DS} in (1). This modification has form:

$$R_{eq} \cong \left.\frac{V_{GS(off)}^{\ 2}}{I_{DSS}\left(V_{set}-2V_{GS(off)}\right)}\right|_{R_a=R_b=R}. \quad (3)$$

The values of $R_{a,b}$ should be several times (100 kΩ) larger than expected channel resistance R_{eq}. However, the range of resistance adjustability is very narrow.



(a) (b)

Fig. 1. J-FET(N) grounded resistors: a) basic concept, b) modified concept.

B. Optocoupler

Optocouplers, having resistive output port, were very popular in recent works as parts for adjustability and tunability of oscillation frequency and oscillation condition in several types of modern oscillators [11]-[14]. However, types (3WK16341) used in [11]-[14] are quite obsolete and unavailable. The modern type of the optocoupler NSL-32SR3 [15] in Fig. 2 represents quite new device very useful for many applications [16]. These resistive equivalents have quite slow reaction on driving voltage (units of ms) but it is not important issue in adjustable applications (condition for oscillation control [11]-[14]). The resulting form for equivalent resistance is:

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$$R_{OC} \cong 0.2 \cdot \left(\frac{R_m}{V_{OC} - V_{th}} \right) \cong 0.2 \cdot \left(\frac{R_m}{V_{OC} - 1.6} \right). \quad (4)$$

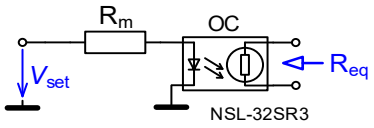


Fig. 2. Optocoupler with resistive output used as floating resistance equivalent.

C. Variable Gain Amplifier

The variable gain amplifier (VGA) [3] in the function of equivalent adjustable resistance offers very useful way and also good linearity. The basic operation supposes resistor connected in the feedback and the variable gain serves for control of overall resistance in the input node (Fig. 3). The resulting equation for overall resistance has form:

$$R_{eq} \cong \frac{R_{ext}}{(1+A)}, \quad (5)$$

for solution in Fig. 3(a) and

$$R_{eq} = R_{ext}(1+A), \quad (6)7$$

for solution in Fig. 3(b). The application of VGA in the resistance equivalent offers simple possibility for negative resistance emulation ($_{\mp} \leftrightarrow \pm$). Unfortunately, instability issues must be solved in the case of negative resistance quite frequently. This solution was used in recent works very effectively [17]-[19]. There are devices that allow linear driving of gain A (VCA822 [20], VCA824 [21]). Exponential driving of voltage gain A ($A = 10^{2(\mathrm{Vset}-1)}$) offers very large range of resistance control in some types of VGA (VCA810 [22] for example).

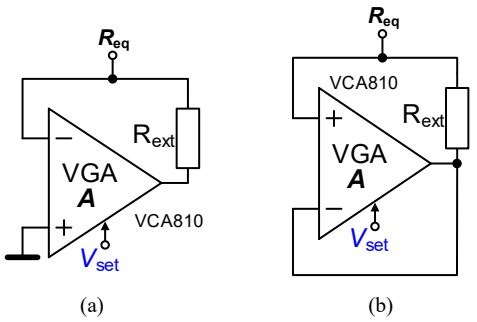


Fig. 3. Grounded equivalent resistance based on variable gain amplifier: a) single feedback, b) two feedbacks.

The voltage-mode multipliers (AD835 [23] for example) also offer very interesting feature for linearly tunable resistance. Typical concept of the controllable resistance is shown in Fig. 4 and has practically identical topology as previous solution using VCA. Therefore, also definition and equation for equivalent resistance has identical form as (5). Again, polarity of R_{ext} connection is not important because of simple change by driving voltage $\pm V_{set}$.

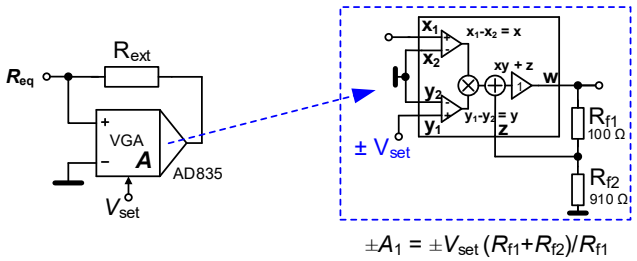


Fig. 4. Grounded equivalent resistance based on variable gain amplifier using voltage-mode multiplier.

III. Analysis of Presented Solutions

Solutions of discussed adjustable resistance circuits are analyzed by computer simulations (PSpice) and experimentally (optocoupler NSL-32SR3 has no model).

A. Simulation of J-FET in linear regime

The simplest method of electronic resistance adjustability, shown in Fig. 1(b), was simulated for BF245A J-FET element [24] using both identical resistors $R_a = R_b = R = 100$ kΩ. and parameters $V_{GS(off)} = -1.8$ V, $I_{DSS} = 4$ mA. The DC driving voltage V_{set} was changed between –1.79 and –0.1 V while resistance varied from 560 up to 211 Ω (theory 450→231 Ω). The analysis in Fig. 5 indicates DC behavior and limits of linearity (up to ±1.8 mA for maximum 560 Ω). Frequency features of the impedance are analyzed in Fig. 6 (good performance up to 10 MHz approximately – flat response). The dependence of resistance on driving parameter (R_{eq} vs V_{set}) is indicated in Fig. 7.

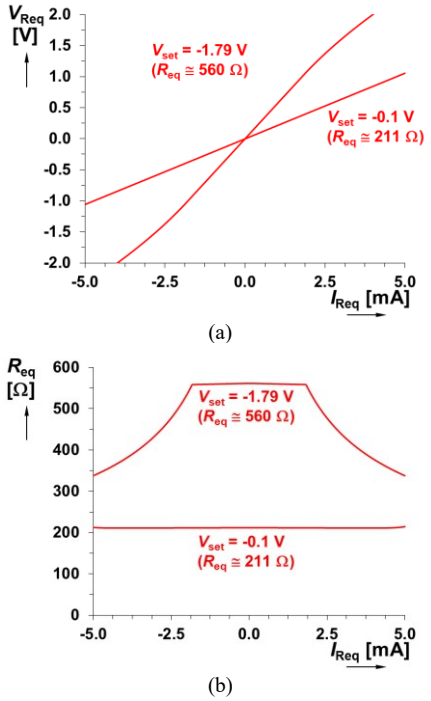


Fig. 5. J-FET-based resistor analysis: a) voltage across element vs current trough element, b) resistance in dependence on current trough element.

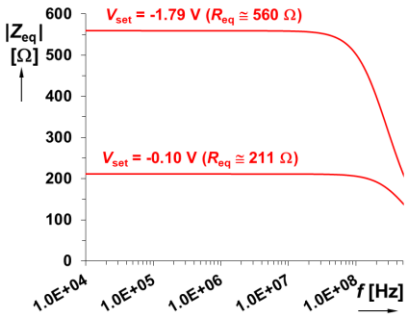


Fig. 6. Frequency responses of impedance magnitude (J-FET).

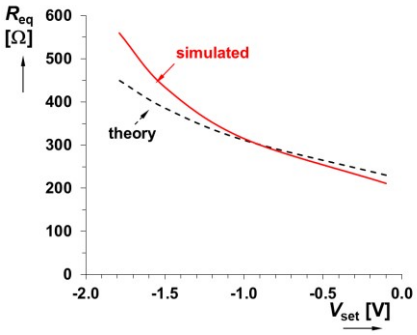


Fig. 7. J-FET Dependence of resistance on driving voltage (J-FET).

B. *Measurement of optocoupler*

The device NSL-32SR3 [15] in Fig. 2 was experimentally tested for parameters: $R_m = 2.2$ kΩ, $V_{set} = 1.62 \rightarrow 5$ V. The R_{eq} varied between 15 kΩ and 160 Ω (22 kΩ → 127 Ω theoretically). Resulting behavior in DC domain indicates excellent performance in dynamics and linearity (Fig. 8) in wide range (more than ±30 mA) for $R_{eq} = 160$ Ω. Flatness of impedance magnitude frequency responses (Fig. 9) is observable up to 500 kHz ($R_{eq} = 15$ kΩ). Figure 10 shows the dependence of R_{eq} on V_{set}.

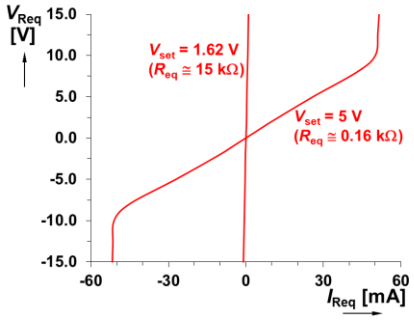


Fig. 8. Voltage across the optocoupler element vs current through element.

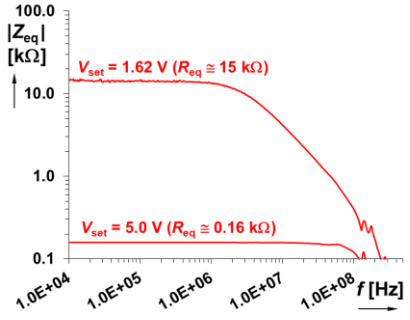


Fig. 9. Frequency responses of impedance magnitude (optocoupler).

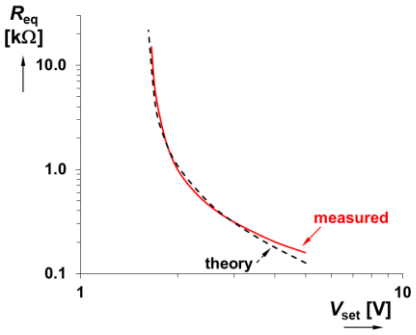


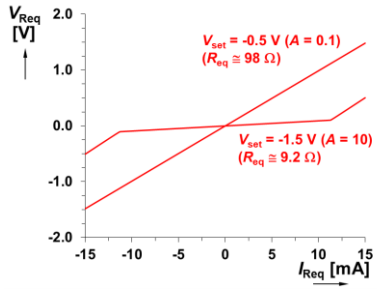
Fig. 10. Dependence of resistance on driving voltage (optocoupler).

C. *Simulation of Variable Gain Amplifier Based Resistance*

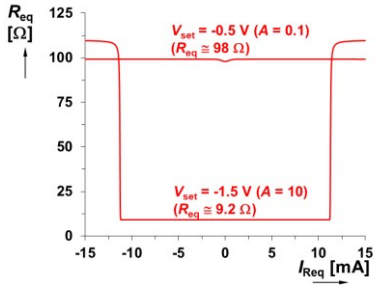
Tests of VGA using VCA810 [22] in adjustable resistor (Fig. 3(a)) bring results valid for $R_{ext} = 100$ Ω and variation of $V_{set} = -0.5 \rightarrow -1.5$ V. Dynamics with good linearity restricts into the range ± 10 mA (Fig. 11) with flat magnitude up to 10 MHz (Fig. 12) and adjustability of resistance R_{eq} in Fig. 13 between 98 and 9.2 Ω (91 → 9.1 Ω theoretically).

The second version of the circuit in Fig. 3(b) allows narrower range of good linearity (Fig. 14) than solution in Fig. 3(a), approximately only ±1 mA for $R_{eq} = 1.2$ kΩ ($V_{set} = -1.5$ V). Frequency features show flat magnitude up to 3 MHz (Fig. 15). Adjustability of R_{eq} was tested between 0.12 and 1.2 kΩ (0.11 → 1.1 kΩ theoretically), see Fig. 16.

Two previous solutions used exponentially adjustable gain. However, the linear driving of gain can be also interesting. The typical modern device known as voltage-mode multiplier AD835 [23] was selected for these purposes (Fig. 4). The value of $R_{ext} = 100$ Ω was applied also in this case but driving voltage V_{set} was adjusted from 0.1 up to 1 V. Figure 17 illustrates better width of linearity than previous case (± 5 mA) for very similar range of R_{eq} between 0.19 and 0.9 kΩ (0.2 → 1.1 kΩ in theory). Frequency features in Fig. 18 show constant R_{eq} value up to 200 kHz. Dependence of R_{eq} on V_{set} is given in Fig. 19.



(a)



(b)

Fig. 11. The first VGA-based resistor analysis : a) voltage across element vs current trougth element, b) resistance in dependence on current trougth element.

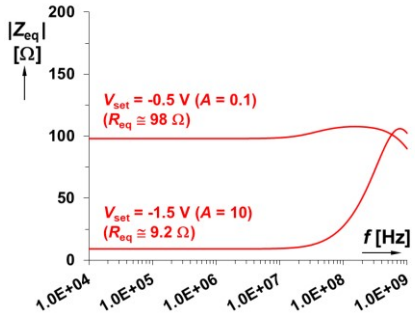


Fig. 12. Frequency responses of impedance magnitude (first VGA-based resistor).

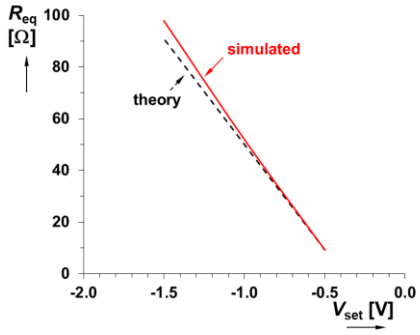
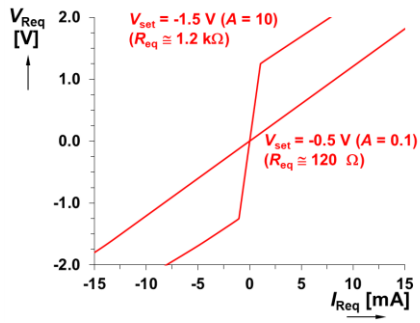
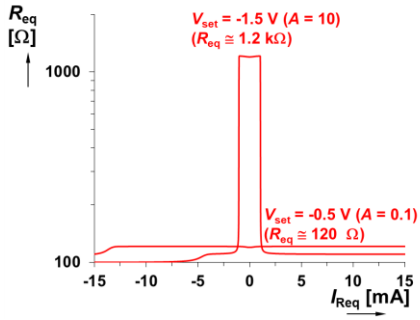


Fig. 13. Dependence of resistance on driving voltage (first VGA-based resistor).



(a)



(b)

Fig. 14. The second VGA-based resistor analysis : a) voltage across element vs current trougth element, b) resistance in dependence on current trougth element

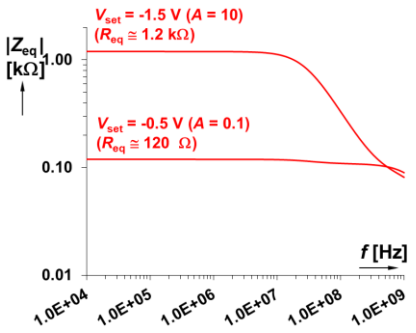


Fig. 15. Frequency responses of impedance magnitude (second VGA-based resistor).

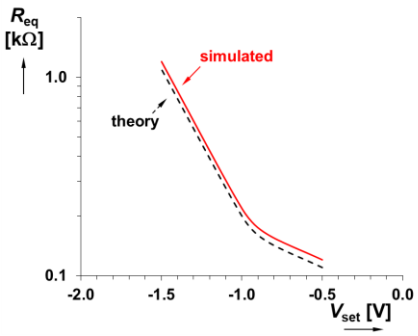
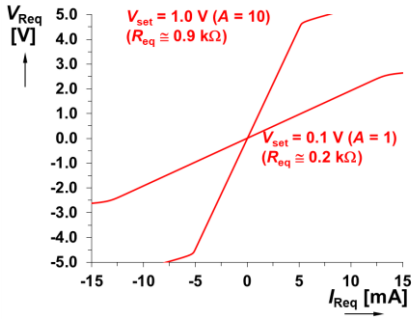
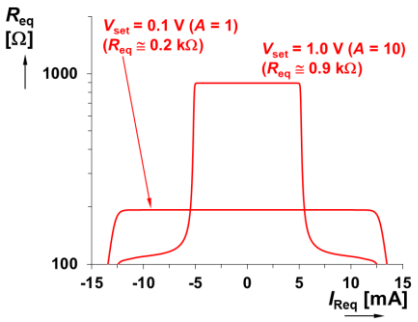


Fig. 16. Dependence of resistance on driving voltage (second VGA-based resistor).



(a)



(b)

Fig. 17. Voltage-mode multiplier-based resistor analysis : a) voltage across element vs current trougth element, b) resistance in dependence on current trougth element.

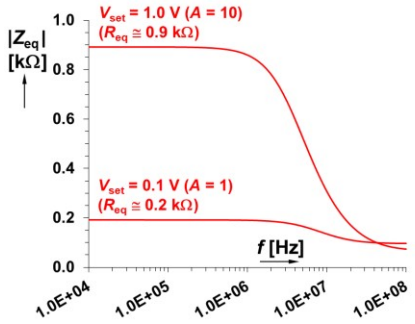


Fig. 18. Frequency responses of impedance magnitude (voltage-mode multiplier-based resistor).

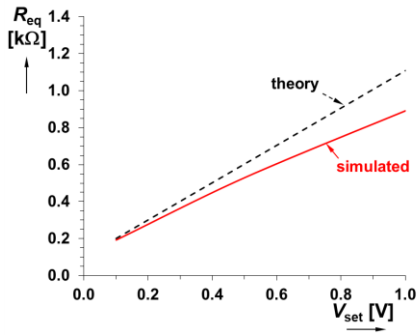


Fig. 19. Dependence of resistance on driving voltage (voltage-mode multiplier-based resistor).

TABLE I. COMPARISON OF STUDIED SOLUTIONS

Type	R_{eq} range [kΩ]	V_{set} range [V] (absolute)	Ratio (R_{eq_max}/R_{eq_min} : V_{set_max}/V_{set_min})	Frequency limit [MHz]	Linear range [mA]
Fig. 1(b)	0.21→0.56	0.1→1.8	0.15	10	±1.8
Fig. 2	15→0.16	1.62→5	30	0.5	±30
Fig. 3(a)	0.098→0.009	0.5→1.5	3.6	10	±10
Fig. 3(b)	0.12→1.2	0.5→1.5	3.3	3	±1
Fig. 4	0.19→0.9	0.1→1	0.5	0.2	±5

IV. COMPARISON OF STUDIED SOLUTIONS

All tested types were designed with very similar or identical values of external R_{ext} component (when applicable) in order to ensure very similar conditions for all tests. Table 1 shows comparison of studied solutions from several points of view (R_{eq} range, ratio of readjustability in dependence on applied driving voltage, frequency limitation, and linearity restriction). The conclusions are following. As expected, the J-FET has the narrowest range of R_{eq} control and linearity. Due to the simplicity, the frequency features should be good (about 10 MHz). Both VGA-based equivalent resistors have quite good ratio of readjustability. However, the linear dynamics of the second type (Fig. 3(b)) is very similar to J-FET (Fig. 1(b)) type (the worst one from the studied cases). The best dynamical performances were obtained for optocoupler in Fig. 2 (wide dynamical range of good linearity and readjustability ratio), however, frequency features are almost the worst from studied cases. The optocoupler represents very useful solution for circuit structures using many floating passive resistors. Perfect examples of application are frequency filter [25], oscillator [16].

V. CONCLUSION

Presented results show important findings. Standard MOSFET or J-FET transistors are suitable only for very simple applications where quite narrow range of resistance (even for linearized solution) and quite low signal level (< 500 mV) is processed. However, many standard application work with significantly higher levels (typically more than 500 mV). The very simple way of usage of OTA-based adjustable resistance exists as discussed [2]. The IC design offers promising features when appropriate linearization method can be applied. However, the commercial availability of these devices (OTAs using differential pair) is very limited (two or three active products) and they suffer from bandwidth or linearity issues.

We tested five types of easily available electronically (voltage) adjustable equivalent of resistance operating in dynamics of units-tens of mA and frequency bandwidths in hundreds and units of MHz. These circuits can be used in various applications based on operational amplifiers and other active elements effectively.

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APPENDIX

Curriculum Vitae

Curriculum Vitae

Ing. Ondřej Domanský

Email: domansky.ondrej@gmail.com

EDUCATION AND COURSES

2007 High School
- *4 years study*
- *Střední průmyslová škola Edvarda Beneše, IT technology*

2011 ICT Course
- *ENG – Diploma ICT, Information Communication Technology, module 1*
- *Software: Excel, Word, PowerPoint*

2011 Bachelor's Degree (Bc.)
- *3 years study*
- *Brno University of Technology*
- *Department of Radio Electronics*

2014 Master's Degree (Ing.)
- *2 years study*
- *Brno University of Technology*
- *Department of Radio Electronics*

2016 Doctor of Philosophy (PhD.)
- *8 years study since this day*
- *form of combined study*
- *Brno University of Technology*
- *Department of Radio Electronics*
- *Management of laboratory teaching, computer exercises and numerical exercises of courses Analog Electronic Circuits and Electrical Filters and Electromagnetic Compatibility*
- *Supervision of students' final bachelor theses*

2021 Additional Pedagogical Study
- *2 years study*
- *Aims to provide teachers with a comprehensive pedagogical education for more effective use in the educational process*
- *Brno University of Technology*

WORK EXPERIENCE

2007 - 2015 Service Technician
- *Firm Noel s.r.o., Hodonín*
- *Transition from analogue to digital television broadcasting*
- *Implementation and construction of new ICT cable distributions*

2016 - 2021 Service Technician
- *Firm Sanmina-SCI Czech Republic s.r.o., Brno*
- *Final Quality Tester*

2021 – until this day Teacher
- *Management of laboratory teaching, computer exercises and numerical exercises of courses Electrical Engineering, Electronics and Graphic Systems*

TECHNICAL KNOWLEDGE

- *Complete Microsoft Office package (Word, Excel, PowerPoint, etc.)*
- *Cadence PSpice A/D and Advanced Analysis*
- *CST Studio Microwave & RF Components*
- *ANSYS HFSS*
- *MATLAB*
- *Eagle PCB Cadsoft design program*
- *Knowledge of HTTP, PHP, CSS and marginal knowledge of C++*

LANGUAGES

- *Czech (native), English (level C1)*