Fully Controllable Immittance Converter

Key features

- **OTA-based general impedance converter**
- **Wide range electronic controllability**
- **Parasitics compensation**
- **Low supply voltage**
- **Low power consumption**

Applications

- **Grounded implementation of synthetic immittance**
- **Floating implementation of synthetic immittance**
- **Synthetic Fractors**
- **Impedance emulators**
- **Resonance circuits**
- **Frequency filters**
- **Parasitic impedance compensation circuits**

Description

The FGIC44 is OTA-based immittance converter that enables to implement grounded or floating synthetic impedance – Fractor F – with the order primarily from the range [–4, 4] by means of primitive passive elements: resistors, capacitors, inductors, fractional-order capacitors and/or fractional-order inductors.

Simplified block diagram of FGIC44 is shown in Fig. 1. The core of FGIC44 is represented by seven OTAs: OTA_1 – OTA_7 that together with four external admittances Y_1 – Y_4 connected to pins 22, 24, 26, 28 provide input admittance Y_{IN} (pins 37 and 39) defined as:

$$[Y_{IN}] = \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \frac{Y_2 Y_4}{Y_1 Y_3} \frac{g_{m1} g_{m2} g_{m3} g_{m4}}{g_{m5} g_{m6} g_{m7}} . \quad (1)$$

Electronic controllability of $|Y_{IN}|$, (i.e. of the fractance F) is ensured in a wide range by using the possibility to adjust all transcoductances g_m of the core OTAs by applying DC voltage to pins 4, 5, 6, 7, 8, 9, 10.

To maintain efficient usage of FGIC44, the interconnection between the output of OTA_1 and OTA_7 is to be made as external by interconnecting pins 30 and 31. Such measure was made primarily to follow the fact that for some cases the lower branch represented by OTA_5, OTA_6, OTA_7 and the external admittances Y_2 and Y_4 may behave as classic resistor with resistivity $R = (G_2 G_4)/(g_{m5} g_{m6} g_{m7})$. In such cases it is more efficient a resistor with resistivity R directly to pin 31. The lower branch of the core group is not used in such cases or may serve as another independent immittance converter to implement a grounded admittance Y_{Gr} at the pin 30:

$$Y_{Gr} = \frac{g_{m5} g_{m6} g_{m7}}{Y_2 Y_4} . \quad (2)$$

FGIC44 also provides offset cancelation (pins 17, 18, 19, 20) of specific OTAs of the core circuit. To provide proper operability at very low and high frequencies of the FGIC44, parasitic conductance compensation in all nodes of the core circuit (pins 21, 23, 25, 27, 29, 36, 38) may be used once connecting compensation admittance to relevant nodes of the core circuit. The compensation admittances are implemented as OTA-based negative admittances by OTA_{c2} – OTA_{c7}, those transconductance g_{mc} is electronically adjusted by DC voltage applied to pins 11, 12, 13, 14, 15, 16.

FGIC44 uses identical OTA cells as shown in Fig. 2. The OTA cell consists of two differential voltage summation blocks. The inputs of the first voltage summation block serve as differential voltage inputs of OTA and the inputs of the second voltage summation block are used to apply the control voltage V_{SET}. The outputs of these summation blocks are multiplied mutually and amplified with the constant k resulting in two output currents with the same magnitude but being shifted in phase by 180 deg:

$$i_{OUT1} = i_{OUT2} = k \cdot V_{SET} (v_+ - v_-) , \quad (3)$$

whereas for the transconductance g_m of the OTA it holds:

$$g_m = k \cdot V_{SET} . \quad (4)$$

FGIC44 was designed using 0.18 µm TSMC CMOS technology with ±0.9 V supply voltage and quiescent current of 50 mA. Bias current of 50 µA is applied to pin 40. FGIC44 is in DIL40 package.

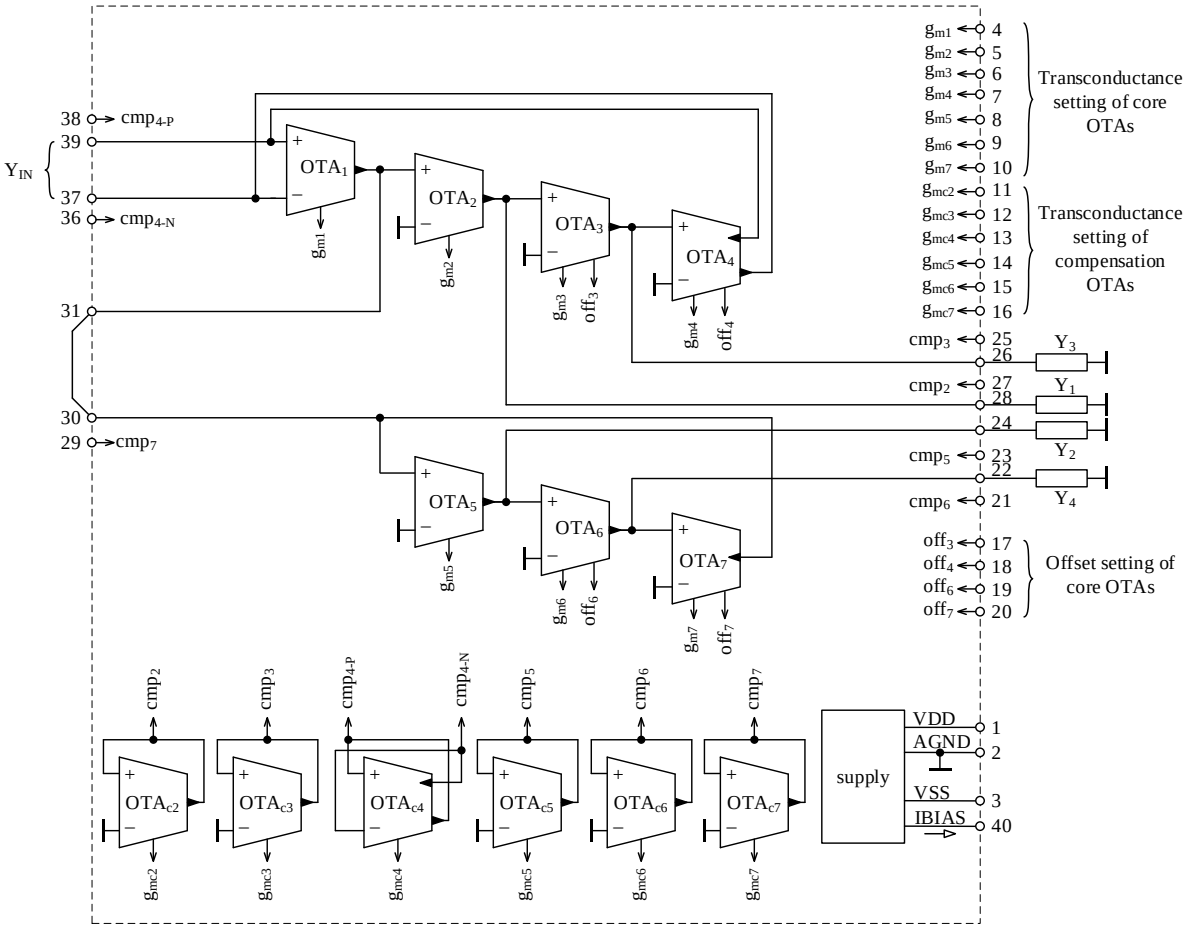


Figure 1. Block diagram of FGIC44

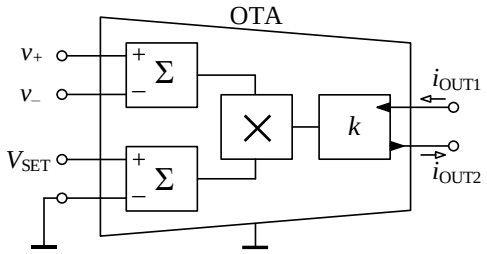


Figure 2. OTA cell used in FGIC44

PIN Configuration

Table 1. Pin description of FGIC44

Pin	Pin description	Pin	Pin description
1	VDD – positive supply voltage	26	Y3 – external admittance Y3
2	AGND – analog ground	27	cmp2 – compensation conductance of OTA_{c2}; to be connected with pin 28
3	VSS – negative supply voltage	28	Y1 – external admittance Y1
4, 5, 6, 7, 8, 9, 10	g_{m1}, g_{m2}, g_{m3}, g_{m4}, g_{m5}, g_{m6}, g_{m7} – transconductance setting of core OTAs	29	cmp7 – compensation conductance of OTA_{c7}; to be connected with pin 30 or 31
11, 12, 13, 14, 15, 16	g_{mc2}, g_{mc3}, g_{mc4}, g_{mc5}, g_{mc6}, g_{mc7} – transconductance setting of compensation OTAs	30	OTA7 – output of lower core circuit; to be connected with pin 31
17, 18, 19, 20	off3, off4, off6, off7 – offset compensation of OTA_3, OTA_4, OTA_6, OTA_7 (core OTAs)	31	OTA1 – output of OTA1
21	cmp6 – compensation conductance of OTA_{c6}; to be connected with pin 22	36	cmp4-N – compensation conductance of OTA_{c4}; to be connected with pin 37
22	Y4 – external admittance Y4	37	YIN-N – “negative” input of FGIC44
23	cmp5 – compensation conductance of OTA_{c5}; to be connected with pin 24	38	cmp4-P – compensation conductance of OTA_{c4}; to be connected with pin 39
24	Y2 – external admittance Y2	39	YIN-P – “positive” input of FGIC44
25	cmp3 – compensation conductance of OTA_{c3}; to be connected with pin 26	40	IBIAS – bias current

Note: Pins not listed in the Table 1 are floating.

Specifications

Vs=±0.9 V, T_A = 25°C, unless otherwise noted

Table 2. Specification of FGIC44

Parameter	Symbol	Min	Typ	Max	Unit
Transconductance setting voltage	V_{SET}	0		0.5	V
Amplification parameter of OTA cell	k		1.46		mAV
Transconductance bandwidth					
@ V_{SET} = 0.1 V	$f_{-3dB-01}$	29.3			MHz
@ V_{SET} = 0.2 V	$f_{-3dB-02}$	26.8			MHz
@ V_{SET} = 0.3 V	$f_{-3dB-03}$	32.2			MHz
@ V_{SET} = 0.4 V	$f_{-3dB-04}$	32.2			MHz
@ V_{SET} = 0.5 V	$f_{-3dB-05}$	35.0			MHz
Trasconductance phase @ 1MHz					
@ V_{SET} = 0.1 V	φ_{01}		–0.92		deg
@ V_{SET} = 0.2 V	φ_{02}		–1.12		deg
@ V_{SET} = 0.3 V	φ_{03}		–1.20		deg
@ V_{SET} = 0.4 V	φ_{04}		–1.21		deg
@ V_{SET} = 0.5 V	φ_{05}		–1.22		deg
Output conductance of core OTAs	G_P	8.65	8.99	9.66	mS
Output capacitance of core OTAs	C_P	8.00	10.16	11.89	pF

Parameters evaluation

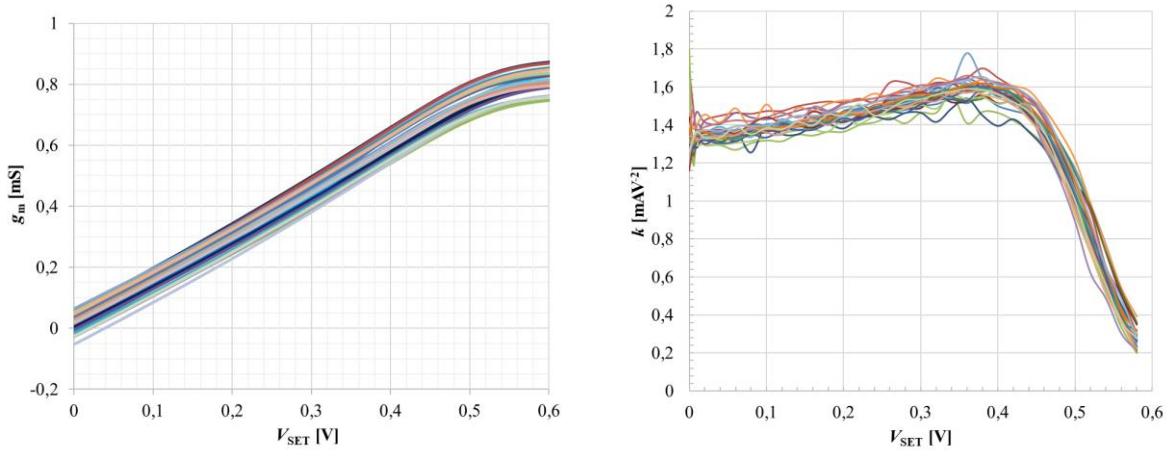
In Fig. 3a, the variation of transconductance g_m of the core OTAs is shown for setting the voltage V_{SET}. The slope of $g_m(V_{SET})$ defines the parameter k that according to (4) results in setting the the transcoducance g_m. Typical value of k is 1.46 (Fig. 3b).

In Fig. 4, the module and phase of transconductance g_m depending on frequency and for selected values of V_{SET} are shown. From the module, the minimum frequency bandwidth as 3dB drop of g_m is 26.8 MHz. For this frequencies, the phase shift is more than –50 dB. Reasonable values of phase shift is up to 1 MHz.

Parasitic conductance G_P at the output of core OTAs is typically 8.99 mS. Parasitic capacitance at the output of core OTAs is typically 10.16 pF. The output impedance of core OTAs is shown in Fig. 5.

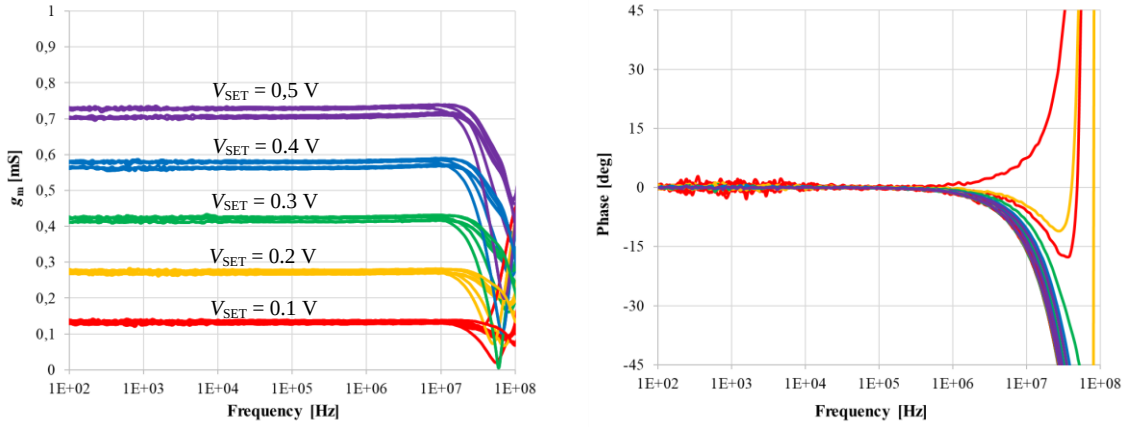
The parasitic conductance G_P may efficiently be compensated by interconnection compensation circuit "cmp" with corresponding node of the core circuit. At compensation pins negative conductance is observed and is connected in parallel with the parasitic conductance G_P. In Fig. 6 a set of plots showing a different level of compensation of the parasitic conductance at different nodes of core circuit. It is obvious that by proper setting of V_{SETcmp} the parasitic conductance G_P may be reduced by two decades. However, it is necessary to prevent overcompensation. As an example, in Fig. 7 the compensation of parasitic conductance G_P at the output of OTA4-N is shown for five values of V_{SETcmp}. Increasing the V_{SETcmp} up to 12.5 mV compensates the G_P, which results in decreasing the output admittance down to 1 µS by keeping the phase of the output admittance at 0 deg at very low frequencies. Increasing the V_{SETcmp} further to 15 mV results in overcompensation primarily visible from Fig. 7b, as the phase of the output admittance at very low frequencies is 180 deg. Hence, the output admittance is negative and may cause instability of FGIC44.

Typical AC and DC Characteristics of FGIC44



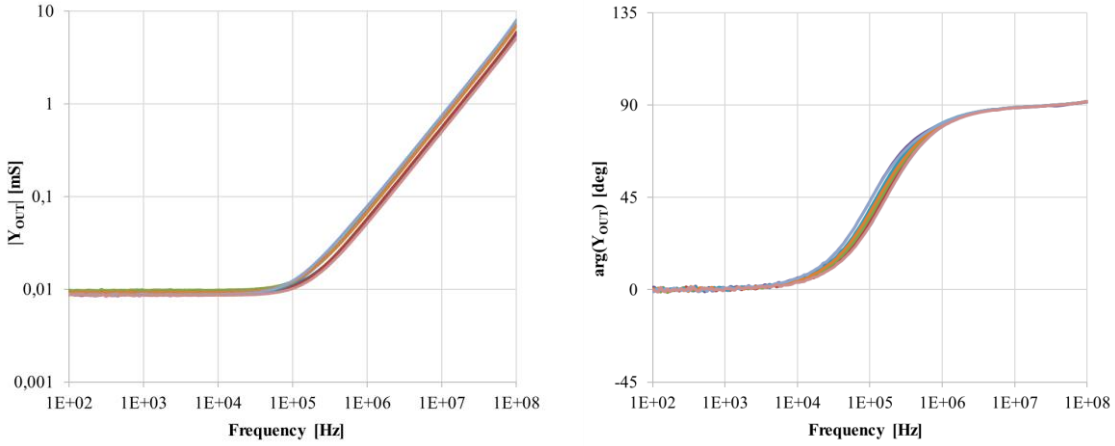
(a) (b)

Figure 3. (a) Transconducnace g_m vs. voltage V_{SET}, (b) k parameter vs. voltage V_{SET} of core OTAs



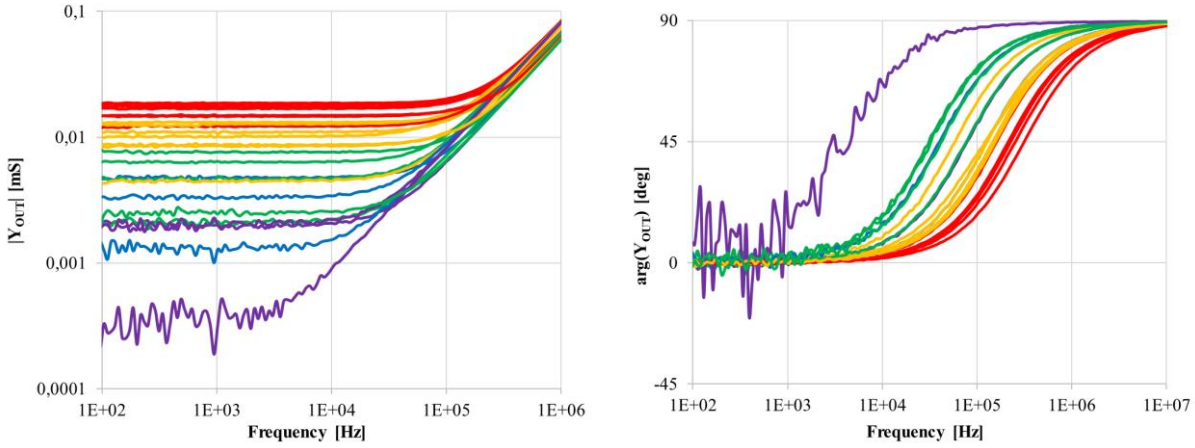
(a) (b)

Figure 4. (a) Modul and (b) phase of the transcoductance g_m vs. voltage V_{SET} of core OTAs



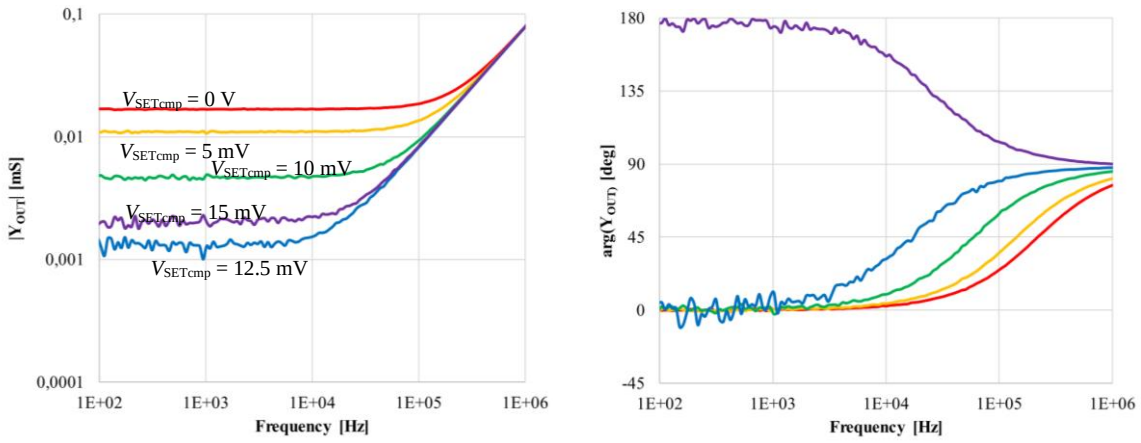
(a) (b)

Figure 5. (a) Modul and (b) phase of output admittance Y_{OUT} of core OTAs (without compensation)



(a) (b)

Figure 6. (a) Modul and (b) phase of output admittance Y_{OUT} of core OTAs (with compensation) for setting V_{SETcmp}



(a) (b)

Figure 7. (a) Modul and (b) phase of output admittance Y_{OUT} of OTA4-N (with compensation) for setting V_{SETcmp}

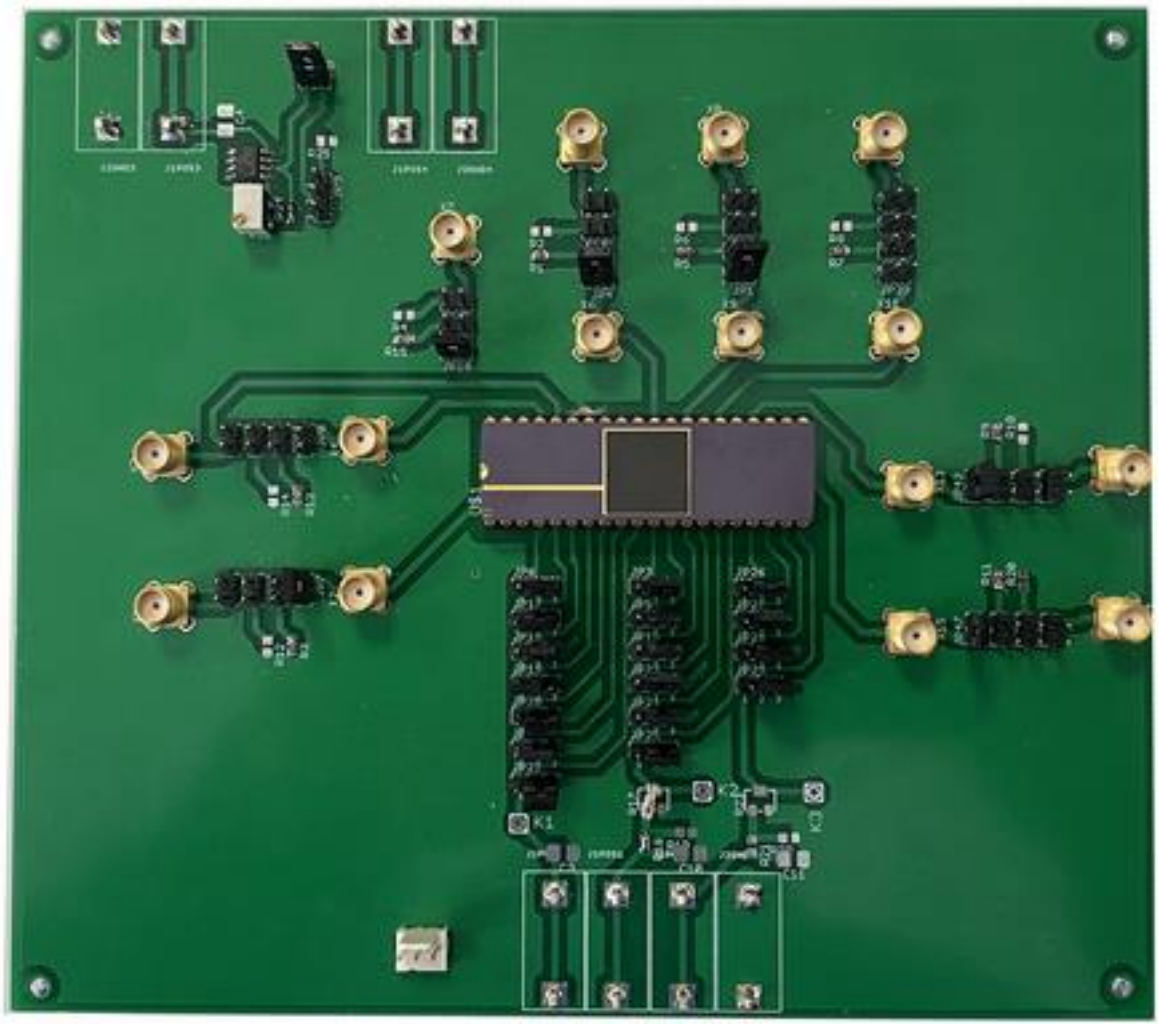
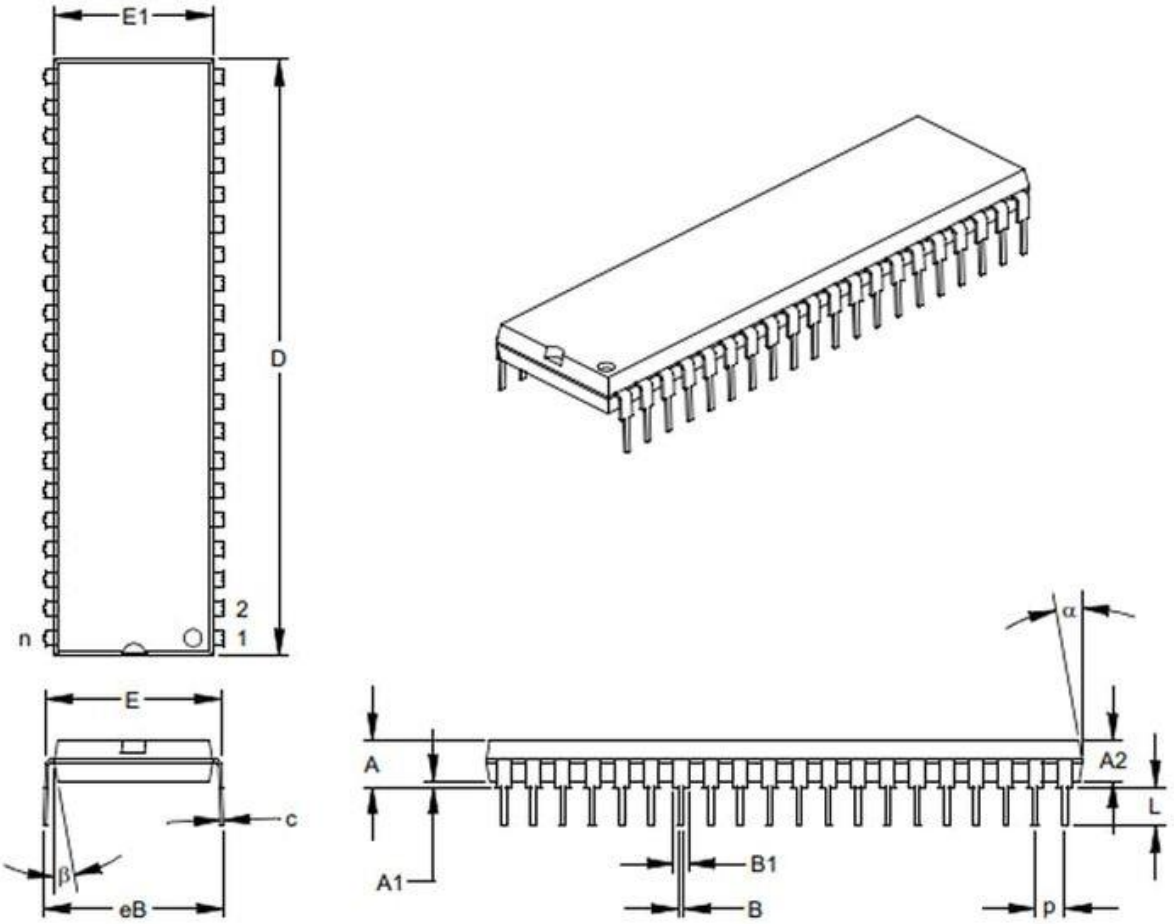


Figure 8. Evaluation board of FGIC44 for DC and AC measurements

Package Information

40-pin DIL



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		40			40	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.160	.175	.190	4.06	4.45	4.83
Molded Package Thickness	A2	.140	.150	.160	3.56	3.81	4.06
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.595	.600	.625	15.11	15.24	15.88
Molded Package Width	E1	.530	.545	.560	13.46	13.84	14.22
Overall Length	D	2.045	2.058	2.065	51.94	52.26	52.45
Tip to Seating Plane	L	.120	.130	.135	3.05	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.030	.050	.070	0.76	1.27	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.620	.650	.680	15.75	16.51	17.27
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15